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=> file reg
FILE 'REGISTRY' ENTERED AT 18:24:25 ON 14 JUN 1999
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=> display history full l1-

     (FILE 'HOME' ENTERED AT 17:50:33 ON 14 JUN 1999)

     FILE 'REGISTRY' ENTERED AT 17:50:46 ON 14 JUN 1999
                E OXYGEN/CN
L1            1 SEA OXYGEN/CN
                E SILICA/CN
L2            1 SEA SILICA/CN
                E SILICON NITRIDE/CN
L3            1 SEA "SILICON NITRIDE"/CN

     FILE 'HCA' ENTERED AT 17:52:17 ON 14 JUN 1999

     FILE 'LCA' ENTERED AT 17:52:26 ON 14 JUN 1999
L4         1236 SEA PATTERN?
L5         1773 SEA L1 OR OXYGENA? OR OZON? OR O2 OR O3 OR (O OR
                OXYGEN#)(2A)(ATMOS? OR ATM# OR GAS## OR GASIF? OR
                GASEOUS? OR TREAT? OR APPLY? OR APPLIED OR APPLICATION?
                OR INJECT? OR INTRODUC?)
L6         3565 SEA OXIDA? OR OXIDN# OR OXIDI?
L7         1939 SEA PLASMA#

     FILE 'HCA' ENTERED AT 17:57:18 ON 14 JUN 1999
L8       141593 SEA ETCH? OR MICROETCH? OR CHASE# OR CHASING# OR ENCHAS?
                OR ENGRAV? OR EMBOSS? OR IMPRINT? OR ENCAUST? OR
                IMPRESS? OR INCISE# OR INCISING#
L9        56952 SEA MASK? OR PHOTOMASK? OR HARDMASK?
L*** DEL   3758 S HARDMASK? OR L9(2N)(HARD? OR (SILICON OR SI)(N)(OXIDE#
L*** DEL  49239 S RESIST OR RESISTS OR PHOTORESIST?
L*** DEL 119906 S ANISOTROP?
L10        3797 SEA HARDMASK? OR L9(2A)(HARD? OR (SILICON OR SI)(A)(OXIDE
                # OR DIOXIDE#) OR SIO2 OR SILICA# OR SIN OR NITRIDE# OR
                OXYNITRIDE# OR L2 OR L3)
L11       49239 SEA RESIST OR RESISTS OR PHOTORESIST?
L12      119906 SEA ANISOTROP?
L13        1806 SEA L8(2A)(STOP? OR HALT?) OR ETCHSTOP? OR MICROETCHSTOP?

L14      175954 SEA DIELEC?
L15       36686 SEA (L5 OR L6) AND L7
L16        4590 SEA L15 AND L8
L17         195 SEA L16 AND L10
L18         321 SEA HARDMASK? OR HARD?(2A)(MASK? OR PHOTOMASK?)
L19          36 SEA L16 AND L18
L20          23 SEA L19 AND L4
L21          28 SEA L19 AND L11
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L22           5 SEA L19 AND L12
L23           1 SEA L19 AND L13
L24           7 SEA L19 AND L14
L*** DEL    195 S L17 AND L8
L25          99 SEA L17 AND L11
L26          10 SEA L25 AND L12
L27           1 SEA L25 AND L13
L28          17 SEA L25 AND L14
L29          55 SEA L25 AND L4
L30          47 SEA L29 AND L5
L31         964 SEA L16 AND L9
L32         579 SEA L31 AND L11
L33         365 SEA L32 AND L4
L34          38 SEA L33 AND L12
L35           6 SEA L33 AND L13
L36          35 SEA L33 AND L14
L37           3 SEA L34 AND L36
L38          28 SEA L22 OR L23 OR L24 OR L27 OR L35 OR L37 OR L26
L*** DEL     23 S (L20 OR L21 OR L26) NOT L38
L39          34 SEA (L20 OR L21 OR L28) NOT L38
L40          23 SEA L38 AND 76/SC,SX
L41           5 SEA L38 NOT L40
L42          28 SEA L39 AND 76/SC,SX
L43           6 SEA L39 NOT L42

=> file hca
FILE 'HCA' ENTERED AT 18:25:03 ON 14 JUN 1999
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=> d l40 1-23 cbib ab hitind

L40  ANSWER 1 OF 23  HCA  COPYRIGHT 1999 ACS
130:290273    ***Anisotropic***     ***plasma***     ***etching***   of
     organic-containing insulating layers in semiconductor device
     fabrication.  Vanhaelemeersch, Serge; Rodionovich, Baklanov Mikhail
     (Interuniversitair Micro-Elektronica Centrum, Belg.).  PCT Int.
     Appl. WO 9921217 A1 19990429, 31 pp.  DESIGNATED STATES: W:  JP, US;
     RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
     PT, SE.  (English).  CODEN: PIXXD2.  APPLICATION: WO 98-BE159
     19981022.  PRIORITY: US 97-63487 19971022; US 98-74524 19980212.
AB   A method for   ***anisotropic***     ***plasma***     ***etching***
     of org.-contg. insulating layers is disclosed.  According to this
     method at least one opening is created in an org.-contg. insulating
     layer formed on a substrate.  These openings are created
     substantially without depositing   ***etch***   residues by
     ***plasma***     ***etching***   said insulating layer in a reaction
     chamber contg. a gaseous mixt. which is composed such that the
     ***plasma***     ***etching***   is highly   ***anisotropic***   .
     Examples of such gaseous mixts. are a gaseous mixt. comprising a
     F-contg. gas and an inert gas, or a gaseous mixt. comprising an
     ***O***  -contg.   ***gas***   and an inert gas, or a gaseous mixt.
     comprising HBr and an additive.  The   ***plasma***
     ***etching***   of the org.-contg. insulating layer can be performed
     using a   ***patterned***   bilayer as an   ***etch***
     ***mask***  , said bilayer comprising a   ***hard***     ***mask***
     layer, being formed on said org.-contg. insulating layer, and a
     ***resist***   layer being formed on said   ***hard***
```

mask layer.
IC ICM H01L021-3065
CC ***76-3*** (Electric Phenomena)
ST ***anisotropic*** ***plasma*** ***etching*** org
insulator semiconductor device fabrication
IT ***Resists***
(Sumitomo i-line; ***anisotropic*** ***plasma***
etching of org.-contg. insulating layers in semiconductor
device fabrication)
IT ***Anisotropic*** ***etching***
Contact holes
Dielectric films
Gaseous mixtures
Plasma ***etching***
Semiconductor device fabrication
(***anisotropic*** ***plasma*** ***etching*** of
org.-contg. insulating layers in semiconductor device
fabrication)
IT Aromatic hydrocarbons, processes
Polyimides, processes
Polymers, processes
(***anisotropic*** ***plasma*** ***etching*** of
org.-contg. insulating layers in semiconductor device
fabrication)
IT Polyethers, processes
(arom.; ***anisotropic*** ***plasma*** ***etching***
of org.-contg. insulating layers in semiconductor device
fabrication)
IT ***Etching*** ***masks***
Photolithography
Reactive ion ***etching***
(in ***anisotropic*** ***plasma*** ***etching*** of
org.-contg. insulating layers in semiconductor device
fabrication)
IT Interconnections (electric)
(vias; ***anisotropic*** ***plasma*** ***etching***
of org.-contg. insulating layers in semiconductor device
fabrication)
IT 124221-30-3, Cyclotene 5021 203945-07-7, SiLK (polymer)
213329-13-6, Flare 2.0
(***anisotropic*** ***plasma*** ***etching*** of
org.-contg. insulating layers in semiconductor device
fabrication)
IT 7664-93-9, Sulfuric acid, processes 155409-97-5, EKC 265
(cleaning soln.; after ***anisotropic*** ***plasma***
etching of org.-contg. insulating layers in semiconductor
device fabrication)
IT 75-10-5, Difluoromethane 75-46-7, Trifluoromethane 75-73-0,
Carbon tetrafluoride 76-16-4, Perfluoroethane 593-53-3,
Monofluoromethane 2551-62-4, Sulfur hexafluoride 7727-37-9,
Nitrogen, uses ***7782-44-7*** , Oxygen, uses 7783-54-2,
Nitrogen trifluoride 10035-10-6, Hydrogen bromide, uses
(***etchant*** ; ***anisotropic*** ***plasma***
etching of org.-contg. insulating layers in semiconductor
device fabrication)
IT 25583-20-4, Titanium mononitride
(in ***anisotropic*** ***plasma*** ***etching*** of
org.-contg. insulating layers in semiconductor device
fabrication)
IT 409-21-2, Silicon monocarbide, processes ***7631-86-9*** ,

Silica , processes 11105-01-4, Silicon ***nitride*** oxide 12033-89-5, Silicon ***nitride*** , processes 39345-87-4, Silicon carbide oxide
(***mask*** ; ***anisotropic*** ***plasma*** ***etching*** of org.-contg. insulating layers in semiconductor device fabrication)

L40 ANSWER 2 OF 23 HCA COPYRIGHT 1999 ACS
130:203747 Method for fabricating tungsten local interconnections in high density CMOS circuits using chromium ***etch*** ***stop*** layer. Kobeda, Edward; Gambino, Jeffrey Peter; Gifford, George Gordon; Mazzeo, Nickolas Joseph (International Business Machines Corporation, USA). U.S. US 5882992 A 19990316, 5 pp., Cont. of U.S. Ser. No. 296,029, abandoned. (English). CODEN: USXXAM. APPLICATION: US 96-751673 19961118. PRIORITY: US 94-296029 19940825.
AB The present invention provides a method for fabricating W local interconnections in high d. CMOS circuits, and also provides high d. CMOS circuits having local interconnections formed of W. Pursuant to the method, an ***etch*** ***stop*** layer of Cr is initially deposited on the circuit elements of the CMOS Si substrate. Next, a conductive layer of W is nonselectively deposited on the Cr layer. A ***photoresist*** ***mask*** is then lithog. ***patterned*** over the W layer. The W layer is then ***etched*** down to, and stopping at, the Cr layer, after which the ***photoresist*** ***mask*** is stripped. The stripping preferably uses a low temp. ***plasma*** ***etch*** in ***O2*** at a temp. of <100.degree.. Finally, a directional ***O2*** reactive ion ***etch*** was used to remove the Cr layer selectively to the Si substrate. Border-less contacts are formed with the aid of the Cr ***etch*** ***stop*** layer beneath the W local interconnection layer. The method of integration of this approach results in anisotropic metal lines ***patterned*** over topog. using a std. ***photoresist*** ***mask*** . This approach also allows partial overlap of contacts to reduce device dimensions, and thereby results in improved d. and performance.
IC ICM H01L021-28
ICS H01L021-4763
NCL 438582000
CC ***76-2*** (Electric Phenomena)
IT Sputter deposition
Vapor deposition process
(chromium; in fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT CMOS devices
Integrated circuits
Interconnections (electric)
SRAM devices
Semiconductor device fabrication
(fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT Electric contacts
Electrically conductive films
Metal lines
Photolithography
Photomasks (lithographic ***masks***)
Reactive ion ***etching***
(in fabricating tungsten local interconnections in high d. CMOS

circuits using chromium ***etch*** ***stop*** layer)
IT ***Plasma*** ***etching***
(oxygen; in fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT 7440-47-3, Chromium, processes
(***etch*** - ***stop*** layer; fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT 7440-33-7, Tungsten, processes
(fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT 7440-21-3, Silicon, processes
(in fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)
IT ***7782-44-7*** , Oxygen, processes
(***plasma*** ***etching*** by; in fabricating tungsten local interconnections in high d. CMOS circuits using chromium ***etch*** ***stop*** layer)

L40 ANSWER 3 OF 23 HCA COPYRIGHT 1999 ACS
130:161253 Study on micromachining by reactive ion ***etching*** .
Norio, Nawachi; Kiyokazu, Toiyama (Western Hiroshima Prefecture Industrial Research Institute, Japan). Hiroshima-kenritsu Seibu Kogyo Gijutsu Senta Kenkyu Hokoku, 41, 9-12 (Japanese) 1998. CODEN: HSGHEM. ISSN: 0915-194X. Publisher: Hiroshima-kenritsu Seibu Kogyo Gijutsu Senta.
AB Reactive ion ***etching*** (RIE) of Si, which was applied to the fabrication to the microstructure, has been studied to develop the microsensor by photo-fabrication. The suitability of SiO2 and ***photoresist*** as the mask material was studied. ***Etch*** rate and selectivity have been examd. as a function of pressure by SF6 ***plasma*** using ***SiO2*** as the ***mask*** material. ***Etch*** profiles in SF6/ ***O2*** gas mixts. were obsd. In result, SiO2 was suitable for the mask material of the ***etching*** in F based ***plasma*** . SF6/ ***O2*** gas mixts. were effective to ***anisotropically*** ***etch*** Si.
CC ***76-3*** (Electric Phenomena)
ST micromachining reactive ion ***etching*** silicon microsensor; ***mask*** ***etching*** ***photoresist*** ***silica*** reactive ion ***etching*** silicon
IT ***Photoresists***
(***etching*** mask; in micromachining of silicon for microsensor by reactive ion ***etching***)
IT ***Anisotropic*** ***etching***
Etching masks
(in micromachining of silicon for microsensor by reactive ion ***etching***)
IT Micromachining
Microsensors
Reactive ion ***etching***
(micromachining of silicon for microsensor by reactive ion ***etching***)
IT 7631-86-9, ***Silica*** , uses
(***etching*** ***mask*** ; in micromachining of silicon for microsensor by reactive ion ***etching***)
IT 7440-21-3, Silicon, processes
(micromachining of silicon for microsensor by reactive ion ***etching***)

IT   2551-62-4, Sulfur fluoride (SF6)   ***7782-44-7***   , Oxygen, uses
        (micromachining of silicon for microsensor by reactive ion
        etching   using)

L40 ANSWER 4 OF 23 HCA COPYRIGHT 1999 ACS
130:146077 Application of   ***plasma***   polymerized methylsilane for
     0.18 .mu.m photolithography. Monget, C.; Lee, C.; Joubert, O.;
     Amblard, G.; Weidman, T. W.; Sugiarto, D.; Yang, J.; Cormont, F.;
     Inglebert, R. L. (CNET/DTM, France Telecom, Meylan, 38243, Fr.).
     Proc. SPIE-Int. Soc. Opt. Eng., 3333(Pt. 1, Advances in Resist
     Technology and Processing XV), 366-375 (English) 1998. CODEN:
     PSISDG. ISSN: 0277-786X. Publisher: SPIE-The International Society
     for Optical Engineering.
AB   ***Plasma***   polymd. methylsilane resist films (PPMS) have high
     sensitivity to short wavelength radiation. The photoinduced
     oxidn . of PPMS films exposed in air forms siloxane network
     material (called PPMSO), allowing dry development by selective
     etching   of the unexposed regions upon treatment with
     chlorine based   ***plasmas*** . Neg.-tone patterns of
     oxidized   methylsilane thus formed can be consolidated in a
     std. resist stripper to form SiO2 like   ***hard***   ***mask***
     patterns. In this work, PPMS films are deposited using a com.
     single wafer cluster tool dedicated to   ***dielec*** . deposition.
     After exposure at 248 or 193 nm, PPMS development is performed in a
     com. high d.   ***plasma***   source   ***etcher*** . Oxide
     patterns obtained from PPMS films are used for org. resist
     patterning (bi-layer application) and gate stack patterning (single
     layer application).
CC   74-5 (Radiation Chemistry, Photochemistry, and Photographic and
     Other Reprographic Processes)
     Section cross-reference(s):   ***76***
ST   photolithog   ***plasma***   polymd methylsilane dry development
     photoresist
IT   ***Plasma***   chemical vapor deposition
       Plasma   polymerization
        (chem. vapor deposition of   ***plasma***   polymd. methylsilane
        photoresist process for deep-UV lithog.)
IT   Photochemical crosslinking
        (***oxidative*** ; photolithog. imaging processes with
        plasma   polymd. methylsilane photoresist)
IT   Photooxidation
     Photoresists
        (photolithog. imaging processes with   ***plasma***   polymd.
        methylsilane photoresist)
IT   Polysiloxanes, processes
        (photolithog. imaging processes with   ***plasma***   polymd.
        methylsilane photoresist)
IT   Polysilanes
        (photolithog. imaging processes with   ***plasma***   polymd.
        methylsilane photoresist)
IT   ***Plasma***   ***etching***
        (***plasma***   ***etching***   selectivity in development
        and stripping steps of photolithog. imaging based on
        poly(methylsilane) photoresist)
IT   992-94-9, Methylsilane
        (chem. vapor deposition of   ***plasma***   polymd. methylsilane
        photoresist process for deep-UV lithog.)
IT   7631-86-9, Silica, processes
        (photolithog. imaging processes with   ***plasma***   polymd.
        methylsilane photoresist)

IT 110477-49-1, Methylsilane homopolymer
(photolithog. processes with ***plasma*** polymd. methylsilane photoresist)
IT 7446-09-5, Sulfur dioxide, processes
(***plasma*** ***etch*** mixt. contg. oxygen and; ***plasma*** ***etching*** selectivity in development and stripping steps of photolithog. imaging based on poly(methylsilane) photoresist)
IT ***7782-44-7*** , Oxygen, processes 7782-50-5, Chlorine, processes 10035-10-6, Hydrogen bromide, processes
(***plasma*** ***etch*** mixt.; ***plasma*** ***etching*** selectivity in development and stripping steps of photolithog. imaging based on poly(methylsilane) photoresist)
IT 75-73-0, Carbon tetrafluoride
(***plasma*** ***etch*** ; ***plasma*** ***etching*** selectivity in development and stripping steps of photolithog. imaging based on poly(methylsilane) photoresist)

L40 ANSWER 5 OF 23 HCA COPYRIGHT 1999 ACS
129:253471 Method of forming and planarizing deep isolation trenches in a silicon-on-insulator (SOI) structure. Yindeepol, Wipawan; McGregor, Joel; Bashir, Rashid; Brown, Kevin; Desantis, Joseph Anthony (National Semiconductor Corp., USA). U.S. US 5811315 A 19980922, 17 pp. (English). CODEN: USXXAM. APPLICATION: US 97-816408 19970313.
AB A method of forming and planarizing a deep isolation trench in a silicon-on-insulator (SOI) structure begins with a base semiconductor substrate, a buried insulator layer formed on the base semiconductor substrate, and an active silicon layer formed on the buried insulator layer. First, an ONO layer is formed on the active silicon layer. The ONO layer includes a layer of field oxide, a first layer of silicon nitride and a layer of deposited ***hardmask*** oxide. A trench having sidewalls that extend to the buried oxide layer is formed. A layer of trench lining oxide is then formed on the exposed sidewalls of the trench. Then, a second layer of silicon nitride is conformably formed on the substrate. The second nitride layer is then ***anisotropically*** ***etched*** to remove the nitride from the exposed horizontal surface of the ***hardmask*** oxide and the buried oxide in the bottom of the trench, but leaving silicon nitride on the vertical sidewall portions of the ***hardmask*** oxide, on the sidewalls of the first nitride layer on the sidewalls of the field oxide and on the trench lining oxide. A layer of polysilicon is then deposited to fill the trench and ***etched*** back such that the top surface of the polysilicon substantially corresponds to the top surface of the layer of field oxide. The ***hardmask*** oxide layer is then removed and the top surface of the polysilicon layer is ***oxidized*** .
IC ICM H01L021-76
NCL 437062000
CC ***76-3*** (Electric Phenomena)
ST SOI substrate trench planarization ***etching***
IT ***Etching***
Plasma ***etching***
(for forming and planarizing deep isolation trenches in a silicon-on-insulator (SOI) structure)
IT 7664-38-2, Phosphoric acid, uses
(***etching*** for forming and planarizing deep isolation trenches in a silicon-on-insulator (SOI) structure with)

L40 ANSWER 6 OF 23 HCA COPYRIGHT 1999 ACS
129:88602 WSi2/poly-Si gate ***etching*** using a TiON ***hard*** ***mask*** . Tabara, Suguru; Hibino, Satoshi; Nakaya, Hiroshi (Process Development Section, Semiconductor Div., YAMAHA Corp., Shizuoka, 438-0192, Japan). Jpn. J. Appl. Phys., Part 1, 37(4B), 2354-2358 (English) 1998. CODEN: JAPNDE. ISSN: 0021-4922. Publisher: Japanese Journal of Applied Physics.

AB The WSi2 ***etch*** selectivity over TiON was high enough in a Cl2/ ***O2*** ***plasma*** to allow the use of TiON as an ***etching*** mask for WSi2/poly-Si gate ***etching*** . The high content of Ti-O bonds in TiON films is assumed to be the reason why TiON films can serve as ***etching*** masks. ***Anisotropic*** ***etching*** down to a line width of 0.06 .mu.m was achieved using TiON thin films as ***etching*** masks. Charging damage from the electron shading effect is avoided by using thin TiON films as ***etching*** masks. In a photolithog. context, improved crit. dimension controllability are expected by adopting an org. antireflecting coating/TiON stacked layer as an antireflecting layer for WSi2/poly-Si gate definition.

CC ***76-3*** (Electric Phenomena)

ST tungsten disilicide polysilicon gate ***plasma*** ***etching***

IT ***Plasma*** ***etching***
(WSi2/poly-Si gate ***etching*** using TiON ***hard*** ***mask***)

IT Electrodes
(gates; WSi2/poly-Si gate ***etching*** using TiON ***hard*** ***mask***)

IT 7440-21-3, Silicon, uses 12039-88-2, Tungsten disilicide
(WSi2/poly-Si gate ***etching*** using TiON ***hard*** ***mask***)

IT 71330-02-4, Titanium nitride oxide (tino)
(WSi2/poly-Si gate ***etching*** using TiON ***hard*** ***mask***)

L40 ANSWER 7 OF 23 HCA COPYRIGHT 1999 ACS
128:277765 A method of forming copper dry ***etch*** ***hardmask*** . Anon. (UK). Res. Discl., 408(April), P389 (No. 40877) (English) 1998. RD 408077 19980410. CODEN: RSDSBB. ISSN: 0374-4353. PRIORITY: RD 98-408077 19980410. Publisher: Kenneth Mason Publications Ltd..

AB A method is disclosed for creating a copper dry ***etch*** ***hardmask*** . The method is also compatible for subtractive copper integration processes. Current processes use Ta or TaN on top of Cu as a protection layer. The Ta or TaN serves as an oxide ***etch*** ***stop*** and will be exposed to the oxygen ***plasma*** and solvent used in the ***resist*** strip step. These processes showed several issues such as corrosion, peeling, and ***oxidn*** . The disclosed processing sequence to form a Cu dry ***etch*** ***hardmask*** is: (1) Cu deposition, (2) SiN deposition, (3) SiO2 deposition, (4) lithog., (5) differential ***etch*** , ***etch*** SiO2 and ***stop*** at SiN, (6) ***resist*** strip, (7) SiN ***etch*** using ***SiO2*** as ***mask*** and stops at Cu. The main benefit of using this approach is that ***resist*** can be removed while Cu is protected by SiN. The SiO2 and SiN thickness can be adjusted to accommodate the integration requirement.

CC ***76-14*** (Electric Phenomena)

ST copper dry ***etch*** ***hardmask*** formation; ***plasma*** ***etch*** ***hardmask*** copper formation

IT ***Plasma*** ***etching***
(***hardmasks*** ; formation of copper dry ***etch*** ***hardmasks***)
IT 7440-50-8, Copper, uses
(***hardmasks*** ; formation of copper dry ***etch*** ***hardmasks***)

L40 ANSWER 8 OF 23 HCA COPYRIGHT 1999 ACS
128:251475 Fabricating stacked capacitors on dynamic random access memory cells. Tseng, Horng-huei (Vanguard International Semiconductor Corp., Taiwan). U.S. US 5731130 A 19980324, 13 pp. (English). CODEN: USXXAM. APPLICATION: US 96-747500 19961112.
AB A method for manufg. an array of stacked capacitors with increased capacitance for DRAM devices uses 2 ***photoresist*** ***masking*** steps and self-aligning ***etchback*** steps to form a very high-d. array of bottom capacitor (node) electrodes. The method involves depositing and planarizing an insulating layer over the DRAM cell areas in which node contact openings (1st ***photoresist*** ***mask***) are ***etched*** to the node contact areas of the FETs. A polysilicon layer is deposited, filling the node contact openings, and ***patterned*** (2nd ***photoresist*** ***mask***) to define the perimeters of the bottom electrodes, and the polysilicon layer is recessed by partial ***plasma*** ***etching*** . The 2nd ***patterned*** ***photoresist*** ***mask*** is then laterally recessed by ashing in ***O2*** to expose the polysilicon. A 2nd ***anisotropic*** ***etch*** is used to form a bottom electrode having a vertical center portion and a wider base area. A conformal insulating layer is deposited and ***etched*** back to form sidewall spacers followed by a polysilicon deposition and ***etchback*** to form vertical portions on the electrode. The capacitors are then completed by removing (***etching***) the spacer and portions of the planar underlying layer and forming an interelectrode ***dielec*** . on the bottom electrodes and ***patterning*** another polysilicon layer to form the top electrodes.
IC ICM B03C005-00
ICS H01L021-70
NCL 430316000
CC ***76-3*** (Electric Phenomena)
IT ***Anisotropic*** ***etching***
Ashing
Etching
Photoresists
Plasma ***etching***
(in fabricating stacked capacitors on DRAM cells)

L40 ANSWER 9 OF 23 HCA COPYRIGHT 1999 ACS
127:27536 Manufacture of semiconductor device by improved diffusion-enhanced silylating ***resist*** process. Nasu, Masaaki; Adachi, Koichiro; Fujimoto, Koji (Sharp Corp., Japan). Jpn. Kokai Tokkyo Koho JP 09106938 A2 19970422 Heisei, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 95-263903 19951012.
AB The manufg. process includes these steps; exposing a ***resist*** -coated semiconductor substrate through a mask, supplying a SiH3-contg.compd. to silylate the exposed part selectively, irradiating the ***resist*** surface with O ***plasma*** to hydrophilize the silylated part, growing SiO2 on the hydrophilized part using H2SiF6 aq. soln., and developing the ***resist*** through the ***SiO2*** ***mask*** by ***anisotropic***

dry ***etching*** . The process provides small-dimension patterns.
IC ICM H01L021-027
ICS G03F007-20; G03F007-38; H01L021-3065
CC ***76-3*** (Electric Phenomena)
ST semiconductor photolithog diffusion enhanced silylating ***resist*** ; silylated ***resist*** ***silica*** growth ***etching*** ***mask*** ; hydrofluorosilicic acid silica growth semiconductor photolithog
IT Photolithography
Semiconductor devices
(improved diffusion-enhanced silylating ***resist*** process for semiconductor device using hydrofluorosilicic acid)
IT 7631-86-9P, ***Silica*** , processes
(***etching*** ***mask*** ; improved diffusion-enhanced silylating ***resist*** process for semiconductor device using hydrofluorosilicic acid)
IT 16961-83-4, Hydrofluorosilicic acid
(improved diffusion-enhanced silylating ***resist*** process for semiconductor device using hydrofluorosilicic acid)
IT 999-97-3, Hexamethyldisilazane
(improved diffusion-enhanced silylating ***resist*** process for semiconductor device using hydrofluorosilicic acid)
IT ***7782-44-7*** , Oxygen, uses
(***plasma*** ; improved diffusion-enhanced silylating ***resist*** process for semiconductor device using hydrofluorosilicic acid)

L40 ANSWER 10 OF 23 HCA COPYRIGHT 1999 ACS
126:270767 Fabrication and characterization of Si-Ge based in-plane-gate transistors. Koester, T.; Stein, J.; Hadam, B.; Gondermann, J.; Spangenberg, B.; Roskos, H. G.; Kurz, H.; Holzmann, M.; Riedinger, M.; Abstreiter, G. (Institut fuer Halbleitertechnik II, Rheinisch-Westfaelische Technische Hochschule Aachen, Sommerfeldstr. 24, Aachen, 52074, Germany). Microelectron. Eng., 35(1-4, Micro- and Nano-Engineering 96), 301-304 (English) 1997. CODEN: MIENEF. ISSN: 0167-9317. Publisher: Elsevier.
AB The authors present an in-situ technol. for fabrication of barrier structures in modulation-doped Si/Si-Ge in-plane-gate (IPG) transistors. A special multilayer- ***resist*** system is developed for pattern transfer by electron-beam lithog. (EBL) and ***anisotropic*** SF6/ ***O2*** dry ***etching*** . Barriers are realized by ***etch*** -trenches cutting the two dimensional electron gas (2DEG). The trenches are filled up with a low temp. remote ***plasma*** enhanced CVD (RPECVD) or SiO2. Dry- ***etching*** and passivation are done in-situ to avoid contamination. IPG transistors with different geometric dimensions were fabricated and elec. characterized. Transistor operation is demonstrated up to T = 77 K. The breakdown voltage and the depletion length of the devices were estd. The data indicate the advantage of this in-situ technol. in comparison to other fabrication techniques.
CC ***76-3*** (Electric Phenomena)
Section cross-reference(s): 74
ST silicon germanium in plane gate transistor; electron beam lithog silicon germanium transistor; dry ***etching*** silicon germanium transistor; titanium ***mask*** ***silica*** ***etching*** transistor
IT Electron beam lithography
Passivation

Plasma   chemical vapor deposition
Plasma   ***etching***
Reactive ion   ***etching***
(in fabrication of silicon-germanium based in-plane-gate transistors)
IT 2551-62-4, Sulfur fluoride (SF6)   ***7782-44-7*** , Oxygen, processes
(dry ***etchant*** ; in fabrication of silicon-germanium based in-plane-gate transistors)
IT 75-46-7
(silica ***plasma***   ***etchant*** ; in fabrication of silicon-germanium based in-plane-gate transistors)

L40 ANSWER 11 OF 23 HCA COPYRIGHT 1999 ACS
126:13447 Fabrication of dual-damascene structures in low ***dielectric*** constant polymers for multilevel interconnects. Tacito, r.; Steinbruchel, C. (Dep. Mater. Sci. Eng., Rensselaer Polytech. Inst., Troy, NY, 12180, USA). Mater. Res. Soc. Symp. Proc., 427(Advanced Metallization for Future ULSI), 449-454 (English) 1996. CODEN: MRSPDH. ISSN: 0272-9172. Publisher: Materials Research Society.
AB Parylene-n (pa-n) and benzocyclobutene (BCB) are novel candidate materials for interlevel ***dielecs*** . in future multilevel interconnects, due to their ***dielec*** . const. being much lower than that of silicon dioxide. We describe the fine line patterning of these materials by reactive ion ***etching*** in ***O2*** /CF4 ***plasmas*** . Examples of high aspect ratio trenches and dual damascene structures are presented involving processes with single and double ***hard***   ***masks*** .
CC ***76-3*** (Electric Phenomena)
IT ***Dielectric*** constant
Electric insulators
Interconnections (electric)
Lithography
Sputter ***etching***
(fabrication of dual-damascene structures in low ***dielec*** . const. polymers for multilevel interconnects)
IT 75-73-0 ***7782-44-7*** , Oxygen, processes 25722-33-2, Parylene-n 124221-30-3
(fabrication of dual-damascene structures in low ***dielec*** . const. polymers for multilevel interconnects)

L40 ANSWER 12 OF 23 HCA COPYRIGHT 1999 ACS
125:288582 Mix-and-match lithography processes for 0.1 .mu.m MOS transistor device fabrication. Yew, Jen-Yu; Chen, Lih-Juann; Nakamura, Kazumitsu; Chao, Tien-Sheng; Lin, Horng-Chih (Department Materials Science and engineering, National Tsing Hua University, Hsinchu, 30043, Taiwan). Proc. SPIE-Int. Soc. Opt. Eng., 2723(Electron-Beam, X-Ray, EUV, and Ion-Beam Submicrometer Lithographies for Manufacturing VI), 180-188 (English) 1996. CODEN: PSISDG. ISSN: 0277-786X.
AB The mix-and-match method is an effective method to meet the requirements of minimizing the exposure time and the feature size, in which only the crit. gate layer is exposured by electron beam lithog. system, and the other ones by conventional g-line stepper. The neg. type chem. amplified ***resist*** SAL601, made by Shipley, has been used for gate fabrication. The optimum conditions for the electron beam lithog. including mark dimension, ***resist*** process and ***etching*** process have been investigated. The accelerating voltage and the beam current were

fixed to be 40 kV and 0.25 nA, resp. The mark of the electron beam lithog. has the trench cross shape of 0.5 .mu.m in depth, 20 .mu.m in length and 3 .mu.m in width. The sensitivity of SAL601 ***resist*** has been 20 .mu.C/cm2 for 0.1 .mu.m patterning at 40 kV accelerating voltage. The polysilicon gate was ***etched*** by electron cyclotron resonance (ECR) with ***SiO2*** thin ***mask*** in HBr/ ***O2*** gas, for the appropriate ***anisotropy*** of ***etching*** and for the polysilicon-to-oxide selectivity of HBr/ ***O2*** gas ***plasma*** . The well defined profile of polysilicon gate with 0.1 .mu.m width has been obtained successfully.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): ***76***

IT ***Etching***
Transistors
(electron-beam lithog. for fabrication of 0.1 .mu.m MOS transistor device)

IT 75-46-7, Trifluoromethane 75-73-0, Carbon tetrafluoride ***7782-44-7*** , Oxygen, processes 10035-10-6, Hydrogen bromide, processes
(***etchant*** ; electron-beam lithog. for fabrication of 0.1 .mu.m MOS transistor device)

IT 119574-53-7, SAL 601
(***resist*** ; electron-beam lithog. for fabrication of 0.1 .mu.m MOS transistor device)

L40 ANSWER 13 OF 23 HCA COPYRIGHT 1999 ACS

125:209605 Patterning of benzocyclobutene by reactive ion ***etching*** . Tacito, Robert D.; Steinbruchel, Christoph (Mater. Eng. Dep. Cent. Int. Electron. Electron. Manufacturing, Rensselaer Polytech. Inst., Troy, NY, 12180, USA). J. Electrochem. Soc., 143(8), 2695-2697 (English) 1996. CODEN: JESOAN. ISSN: 0013-4651.

AB This work focuses on the fine-line patterning of benzocyclobutene (BCB), a silicon contg., thermoset polymer for potential application as an interlayer ***dielec*** . (ILD) in multilevel metalization. ***Etch*** rates for BCB have been detd. in ***plasmas*** contg. mixts. of ***O2*** and CF4. Conditions needed to optimize the patternability of BCB have been detd. with respect to ***etch*** rates and trench sidewall profiles. A trilevel system consisting of an imaging layer, a barrier layer (***hard*** ***mask***), and the polymer ILD has been employed to fabricate submicron trenches and inlayed structures of the dual damascene type. Effects of ***plasma*** treatment on the surface of BCB are also reported.

CC ***76-3*** (Electric Phenomena)
Section cross-reference(s): 38, 74

ST benzocyclobutene siloxane polymer photoresist ***plasma*** ***etching***

IT Siloxanes and Silicones, processes
(benzocyclobutene group contg.; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)

IT Electric insulators and ***Dielectrics***
(interlayer, for IC interconnects; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)

IT Kinetics of ***etching***
(patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)

IT Sputtering
(***etching*** , reactive, patterning of benzocyclobutene

siloxane polymer by reactive ion ***etching***)
IT Electric circuits
(integrated, patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT Electric conductors
(interconnections, ***dielec*** . for; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT ***Etching***
(sputter, reactive, patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT Lithography
(submicron, patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT 75-73-0 ***7782-44-7*** , Oxygen, processes
(***etchant*** ; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT 7440-21-3, Silicon, processes
(integrated circuits; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT 7440-50-8, Copper, processes
(interconnects; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT 124221-30-3, BCB
(interlayer ***dielec*** .; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)
IT 7631-86-9, Silica, processes
(masks; patterning of benzocyclobutene siloxane polymer by reactive ion ***etching***)

L40 ANSWER 14 OF 23 HCA COPYRIGHT 1999 ACS
122:227765 Fabrication and characterization of Si/Si-Ge nanometer structures. Gondermann, J.; Spangenberg, B.; Koester, T.; Hadam, B.; Roskos, H. G.; Kurz, H.; Brunner, J.; Schittenhelm, P.; Abstreiter, G.; et al. (Institut fuer Halbleitertechnik II, Rheinisch-Westfaelische Technische Hochschule Aachen, Sommerfeldstr. 24, Aachen, 52074, Germany). Microelectron. Eng., 27(1-4), 83-6 (English) 1995. CODEN: MIENEF. ISSN: 0167-9317.
AB The authors study two different techniques for fabrication of nanometer structures in the Si/Si-Ge system. The additive approach is based on local MBE through micro-shadow masks with lateral dimensions down to 200 nm. Mesas of high cryst. quality are achieved because of the fact that the mesas are not in touch with the surrounding mask material. The authors observe clear excitonic emission from the Si-Ge wires. The subtractive technique combines high-resoln. electron-beam lithog. with reactive-ion- ***etching*** pattern transfer. The ***anisotropic*** process is based on SF6/ ***O2*** - ***plasma*** ***etching*** at a reduced substrate temp. of -20.degree.. The authors fabricate structures with lateral widths from 4 .mu.m down to 50 nm. Photoluminescence is detected for structures .gtoreq.400 nm.
CC ***76-3*** (Electric Phenomena)
IT Sputtering
(***etching*** , fabrication of nanometer structures in Si/Si-Ge system)
IT ***Etching***
(sputter, fabrication of nanometer structures in Si/Si-Ge system)
IT 7631-86-9, ***Silicon*** ***dioxide*** , processes
12033-89-5, Silicon ***nitride*** , processes
(***mask*** ; fabrication of nanometer structures in Si/Si-Ge

system)
IT 2551-62-4, Sulfur fluoride (SF6) ***7782-44-7*** , Oxygen, processes
(***plasma*** ***etchant*** ; fabrication of nanometer structures in Si/Si-Ge system)
IT 7440-32-6, Titanium, processes 9011-14-7, PMMA 123338-25-0, AZ5206
(***resist*** system; fabrication of nanometer structures in Si/Si-Ge system)
IT 75-46-7, Fluoroform
(silicon nitride ***etchant*** ; fabrication of nanometer structures in Si/Si-Ge system)
IT 10294-34-5, Boron trichloride
(titanium ***etchant*** ; fabrication of nanometer structures in Si/Si-Ge system)

L40 ANSWER 15 OF 23 HCA COPYRIGHT 1999 ACS
122:227763 10-nm Silicon lines fabricated in (110) silicon. Namatsu, H.; Nagase, M.; Kurihara, K.; Iwadate, K.; Murase, K. (NTT LSI Laboratories, 3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa, 243-01, Japan). Microelectron. Eng., 27(1-4), 71-4 (English) 1995. CODEN: MIENEF. ISSN: 0167-9317.
AB A technique which satisfies both high resoln. and min. linewidth fluctuation was developed for fabrication of nanometer-scale Si structures. The technique is based on the development of ***resist*** with hexyl acetate and the ***anisotropic*** ***etching*** of Si with KOH. The combination of ZEP-520 ***resist*** and hexyl acetate developer is effective to improve the resoln. and reduce pattern fluctuation in e-beam lithog. ***Resist*** lines <20nm wide with a fluctuation <3nm were obtained. When these lines, aligned in the .ltbbrac.112.rtbbrac. direction on a (110) Si wafer by using the fan-pattern method, are transferred to Si by KOH ***etching*** , linewidth fluctuation is reduced further because the (111) planes form the sidewalls. A feature size .gtoreq.7nm can be formed by addnl. ***etching*** using alc.-added KOH soln.
CC ***76-3*** (Electric Phenomena)
Section cross-reference(s): 74
ST silicon line ***etching*** ***resist*** development
IT ***Etching***
Photographic developers
(10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)
IT 142-92-7, Hexyl acetate 1310-58-3, Potassium hydroxide (KOH), processes 136841-46-8, ZEP-520
(10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)
IT 7440-21-3, Silicon, processes
(10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)
IT 67-63-0, 2-Propanol, processes
(KOH ***etchant*** additive; 10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)
IT ***7631-86-9*** , ***Silica*** , processes
(***mask*** ; 10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)
IT ***7782-44-7*** , Oxygen, processes
(***plasma*** ***etchant*** ; 10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and

KOH ***etching***)
IT 628-63-7, Amyl acetate 1330-20-7, Xylene, processes
(***resist*** developer; 10-nm lines fabricated in (110) silicon by hexyl acetate ***resist*** development and KOH ***etching***)

L40 ANSWER 16 OF 23 HCA COPYRIGHT 1999 ACS
122:120064 Deep trenches in silicon using ***photoresist*** as a mask. Cabruja, E.; Schreiner, M. (Centre Nacional de Microelectronica, Campus Universitat Autonoma de Barcelona, Bellaterra, Barcelona, 08193, Spain). Sens. Actuators, A, 37-38(1-6), 766-71 (English) 1993. CODEN: SAAPEB. ISSN: 0924-4247.
AB Si reactive ion ***etching*** using ***photoresist*** as a mask and SF6/C2ClF5-based ***plasma*** was studied. The ***anisotropy*** is believed to be due to a film-passivation mechanism taking place on the sidewalls of the trenches, combined with a chemisorption of Cl atoms, which inhibits the lateral ***etching*** of the Si substrate. This effect was obsd. only in the presence of the ***photoresist*** in the reactor chamber. Some expts. using ***Si*** ***oxide*** as a ***masking*** material were carried out to confirm this assessment. The obtained profiles showed a significant undercut, thus proving that the passivation phenomena are related to the presence of hydrocarbons in the reactor. Finally, the authors achieved a trench depth of 33 .mu.m, with a selectivity of 6 and a good ***anisotropy*** using thick ***photoresist*** as a masking material.
CC ***76-3*** (Electric Phenomena)
Section cross-reference(s): 74
ST deep trench silicon ***photoresist*** mask RIE
IT Passivation
(deep trenches in Si using ***photoresist*** as mask)
IT Sputtering
(***etching*** , deep trenches in Si using ***photoresist*** as mask)
IT ***Etching***
Kinetics of ***etching***
(sputter, deep trenches in Si using ***photoresist*** as mask)
IT 7440-21-3, Silicon, uses
(deep trenches in Si using ***photoresist*** as mask)
IT 76-15-3 2551-62-4, Sulfur fluoride (SF6) ***7782-44-7*** , Oxygen, uses 142486-44-0, AZ 4562
(deep trenches in Si using ***photoresist*** as mask)
IT 160902-73-8, AZ 1415
(***photoresist*** ; deep trenches in Si using ***photoresist*** as mask)

L40 ANSWER 17 OF 23 HCA COPYRIGHT 1999 ACS
121:269796 Fabricating tungsten local interconnections in high-density CMOS circuits. Kobeda, Edward; Gambino, Jeffrey Peter; Gifford, George Gordon; Mazzeo, Nickolas Joseph (International Business Machines Corp., USA). Eur. Pat. Appl. EP 613177 A2 19940831, 6 pp. DESIGNATED STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP 94-100576 19940117. PRIORITY: US 93-9511 19930127.
AB An ***etch*** ***stop*** layer of Cr is initially deposited on the circuit elements of the CMOS Si substrate. Next, a conductive layer of W is nonselectively deposited on the Cr layer. A ***photoresist*** ***mask*** is then lithog. ***patterned*** over the W layer. The W layer is then ***etched*** down to, and stopping at, the Cr layer, after which

the ***photoresist*** ***mask*** is stripped. The stripping preferably uses a low-temp. ***plasma*** ***etch*** in ***O2*** at <100.degree.. Finally, a directional ***O2*** reactive ion ***etch*** is used to remove the Cr layer selectively to the Si substrate. Borderless contacts are formed with the aid of the Cr ***etch*** ***stop*** layer beneath the W local interconnection layer. The method of integration of this approach results in anisotropic metal lines ***patterned*** over topog. using a std. ***photoresist*** ***mask*** . This approach also allows partial overlap of contacts to reduce device dimensions, and thereby results in improved d. and performance.

IC ICM H01L021-90
ICS H01L021-321

CC ***76-3*** (Electric Phenomena)

IT Sputtering
(***etching*** , in fabricating tungsten local interconnections in high-d. CMOS circuits)

IT ***Etching***
(sputter, in fabricating tungsten local interconnections in high-d. CMOS circuits)

IT 7440-47-3, Chromium, uses
(***etch*** ***stop*** layer; in fabricating tungsten local interconnections in high-d. CMOS circuits)

L40 ANSWER 18 OF 23 HCA COPYRIGHT 1999 ACS

120:205850 The development of an ***anisotropic*** Si ***etch*** process selective to GexSi1-x underlayers. Shang, L.; Campbell, S. A.; Liu, W. H. (Dep. Electr. Eng., Univ. Minnesota, Minneapolis, MN, 55455, USA). J. Electrochem. Soc., 141(2), 507-10 (English) 1994. CODEN: JESOAN. ISSN: 0013-4651.

AB The development of a technique for ***anisotropically*** ***etching*** silicon on GeSi is described. Wet chem. ***etching*** exhibits a selectivity of nearly 40:1 but is completely isotropic and requires the use of a ***hard*** ***mask*** . The fluorine ***plasma*** process which was reported as having high selectivity was nonreproducible as a result of significant polymeric deposition on the chamber surfaces. The ***etch*** residue was not easily removed in an ***O2*** ***plasma*** and led to a highly resistive contacts. Reactive ion ***etch*** processes using BCl3/Cl2 and SiCl4 were found to ***anisotropically*** ***etch*** the silicon layer, but had poor selectivity to GeSi. By combining a reactive ion ***etch*** at 300 W forward power and 20 mTorr in SiCl4, with a wet chem. dip, an adequate process for selectivity patterning submicron features was obtained.

CC ***76-3*** (Electric Phenomena)

ST ***etching*** selectivity germanium silicon underlayer

IT Semiconductor devices
(***anisotropic*** ***etching*** of silicon in fabrication of, on germanium silicon underlayer)

IT Sputtering
(***etching*** , ion-beam, reactive, of silicon on germanium-silicon alloy underlayers, selectivity of)

IT ***Etching***
(sputter, ion-beam, reactive, of silicon on germanium-silicon alloy underlayers, selectivity of)

IT 10026-04-7, Tetrachlorosilane
(***anisotropic*** ***etching*** of silicon by, with germanium silicide underlayer, selectivities of)

IT 11148-21-3, Germanium silicide

(***anisotropic*** ***etching*** of silicon on underlayer
of, by tetrachlorosilane)

L40 ANSWER 19 OF 23 HCA COPYRIGHT 1999 ACS
120:148636 ***Etching*** on silicon membranes for sub-0.25-.mu.m
x-ray ***mask*** manufacturing. Muller, K. Paul; Eib, Nicholas
K.; Faure, Thomas B. (IBM Technol. Prod., Hopewell Junction, NY,
12533, USA). J. Vac. Sci. Technol., B, 11(6), 2270-4 (English)
1993. CODEN: JVTBD9. ISSN: 0734-211X.
AB A multilayer ***resist*** (MLR) scheme for the manufg. of
sub-0.25-.mu.m x-ray ***masks*** has been developed. MLR
facilitates the generation of high-aspect ratio ***patterns***
by electron beam lithog. and dry ***etching*** . The top three
layers are std. MLR structures: a thin imaging ***resist***
layer, a thin intermediate layer, and a thick org. underlayer.
Sufficiently, thin low-stress tantalum or tungsten was utilized to
provide oxygen reactive-ion ***etching*** resistance. The
following layers are utilized under the MLR stack: thin tantalum or
tungsten ***etch*** ***stop*** layer; a thin gold plating
base; and 2.5-.mu.m silicon membrane. Low image size bias dry
etch processes that were successfully developed and
performed on the thin x-ray ***mask*** membranes using a
specially modified ***Plasma*** -Therm model 720 ***etch***
tool capable of automatically handling x-ray ***masks*** are
described. Studies of membrane surface temp. as a function of
plasma conditions are presented. Dry ***etch***
processing issues that are driven by the uniqueness of processing on
a membrane substrate and by the uniqueness of the x-ray ***mask***
fabrication process are discussed. ***Mask*** ***pattern***
distortion issues assocd. with MLR processing are examd.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and
Other Reprographic Processes)
Section cross-reference(s): ***76***
ST lithog x ray ***photomask*** multilayer ***resist*** ;
silicon membrane ***etching*** x ray ***mask***
IT ***Resists***
(multilayer, in fabrication of x-ray ***masks*** by electron
beam lithog. and dry ***etching***)
IT ***Photomasks***
(x-ray, multilayer ***resist*** in fabrication of, using
electron beam lithog. and dry ***etching***)
IT 75-73-0, Carbon tetrafluoride 2551-62-4, Sulfur hexafluoride
7727-37-9, Nitrogen, uses ***7782-44-7*** , Oxygen, uses
(***plasma*** , dry ***etching*** with, in electron-beam
lithog. fabrication of x-ray ***mask***)
IT 7440-33-7, Tungsten, uses 7440-47-3, Chromium, uses 7440-57-5,
Gold, uses
(x-ray ***mask*** structure contg. silicon membrane and
multilayer ***resist*** and, dry ***etching*** in
electron-beam lithog. fabrication process for)
IT 7440-21-3, Silicon, uses
(x-ray ***mask*** with membrane of, dry ***etching*** in
electron-beam lithog. fabrication process for)

L40 ANSWER 20 OF 23 HCA COPYRIGHT 1999 ACS
106:59942 Contacts for an integrated circuit. (Texas Instruments Inc.,
USA). Jpn. Kokai Tokkyo Koho JP 61184823 A2 19860818 Showa, 8 pp.
(Japanese). CODEN: JKXXAF. APPLICATION: JP 85-212025 19850925.
PRIORITY: US 84-655005 19840926; US 85-769823 19850826.
AB A method for the prepn. of contacts for an integrated circuit

involves the following steps: (1) prepg. an integrated-circuit
structure having a ***dielec*** . including SiO2 on its surface;
(2) forming a ***hard*** ***mask*** (e.g., Si) on the
structure via a spacer layer (e.g., AZ1400-31); and (3) taper
etching the ***dielec*** . using an O-rich ***plasma***
from a mixt. of O and NF3, CF4, C2F6, BF3, SiF4, SF6, and/or their
mixts. to prep. contact holes at an increased rate.

IC ICM H01L021-28
ICS H01L021-302; H01L021-88

CC ***76-3*** (Electric Phenomena)

ST ***plasma*** ***etching*** contact integrated circuit

IT Electric contacts
(***plasma*** ***etching*** for prepn. of, for integrated
circuits)

IT Electric insulators and ***Dielectrics***
(***plasma*** ***etching*** of silica-contg., in prepn.
of contacts for integrated circuits)

IT Sputtering
(***etching*** , of silica-contg. ***dielecs*** ., in
prepn. of contacts for integrated circuits)

IT ***Etching***
(sputter, of silica-contg. ***dielecs*** ., in prepn. of
contacts for integrated circuits)

IT 7631-86-9, Silicon dioxide, uses and miscellaneous
(***dielecs*** ., ***plasma*** ***etching*** in prepn.
of contacts for integrated circuits)

IT 75-73-0, Perfluoromethane 76-16-4, Perfluoroethane 2551-62-4,
Sulfur hexafluoride 7637-07-2, Boron trifluoride, reactions
7782-44-7 , Oxygen, uses and miscellaneous 7783-54-2
7783-61-1, Perfluorosilane
(***etching*** of silica-contg. ***dielecs*** . by
plasma from, in prepn. of contacts for integrated
circuits)

IT 7440-21-3, Silicon, uses and miscellaneous
(masks, in ***plasma*** ***etching*** for prepn. of
contacts for integrated circuits)

IT 94765-55-6, AZ1400-31
(resist spacer, in ***plasma*** ***etching*** for prepn.
of contacts for integrated circuits)

L40 ANSWER 21 OF 23 HCA

102:104515 Gate contacts. (Fujitsu Ltd., Japan). Jpn. Kokai Tokkyo Koho
JP 59167021 A2 19840920 Showa, 4 pp. (Japanese). CODEN: JKXXAF.
APPLICATION: JP 83-41719 19830314.

AB Poly-Si gate contact ***patterns*** are clearly formed on SiO2
by coating with poly-Si, ***resist*** ***masking*** ,
reactive-ion ***etching*** , ***plasma*** depositing a film,
anisotropically ***etching*** so as to leave the
plasma film only on the side walls, ***etching*** off
the exposed poly-Si, and removing the ***plasma*** film.

IC H01L021-302

CC ***76-2*** (Electric Phenomena)
Section cross-reference(s): 74

IT Electric contacts
(polysilicon gates, photolithog. ***patterning*** of)

IT Electric insulators and ***Dielectrics***
(silica, polysilicon gate contact formation on)

IT Sputtering
(***etching*** , of polysilicon gate contact ***patterns***
on silicon)

IT ***Etching***
(ion-beam, reactive, of polysilicon gate contact ***patterns*** on silicon)
IT ***Etching***
(sputter, of polysilicon gate contact ***patterns*** on silicon)
IT 7631-86-9, uses and miscellaneous
(contact ***patterns*** for polysilicon on)
IT 7440-21-3, uses and miscellaneous
(gate contacts from polycryst., photolithog. ***patterning*** of)
IT 74-85-1, uses and miscellaneous 7440-37-1, uses and miscellaneous
(in polysilicon gate contact ***patterning***)
IT ***7782-44-7*** , uses and miscellaneous
(***plasma*** ***etchant*** from carbon tetrachloride and, for ***patterning*** of polysilicon gate contacts)
IT 56-23-5, properties
(***plasma*** ***etchant*** from oxygen and, for ***patterning*** of polysilicon gate contacts)
IT 75-73-0
(reactive-ion ***etchant*** from oxygen and, for polysilicon gate contacts)
IT 67-66-3, uses and miscellaneous
(reactive-ion ***etchant*** from, for ***patterning*** of polysilicon gate contacts)

L40 ANSWER 22 OF 23 HCA COPYRIGHT 1999 ACS
99:167939 Studies of ***plasma*** ***etching*** mechanisms with cantilever structures. Reynolds, John L.; Hollins, Jack B.; Neureuther, Andrew R. (Electron. Res. Lab., Univ. California, Berkeley, CA, 94720, USA). Proc. - Electrochem. Soc., 83-10(Proc. Symp. Plasma Process., 4th), 61-74 (English) 1983. CODEN: PESODO. ISSN: 0161-6374.
AB Cantilevered structures were used to explore the relative importance of factors such as surface migration, ion directionality, and the basic isotropic and ***anisotropic*** components in ***plasma*** ***etching*** . Computer simulation was used to illustrate the various mechanisms that may be expected. Integrated cantilever structures were fabricated by overetching a supporting material (polyimide or SiO2) beneath a noneroding ***mask*** (Ti or ***hardened*** ***resist***). This diagnostic structure was used in studies of Si ***etching*** with SF6/ ***O2*** , CF4/ ***O2*** , and C2F6/ ***O2*** under various powers, pressures and flow rates. No surface migration or angularly distributed effects are found in the exptl. structures. The profiles can be explained by a simple isotropic ***etch*** rate component superimposed upon a well-collimated ion enhanced ***anisotropic*** component. Tables of these components are given as a function of power, pressure and flow-rate.
CC ***76-11*** (Electric Phenomena)
ST silicon ***plasma*** ***etching*** mechanism
IT ***Plasma*** , chemical and physical effects
(***etching*** by, mechanism of, cantilever structures in)
IT Sputtering
(***etching*** , mechanism of, cantilever structures in)
IT ***Etching***
(sputter, mechanism of, cantilever structures in)
IT ***7782-44-7*** , reactions
(***plasma*** ***etching*** by gas mixts. contg., of silicon, mechanism of)

IT 75-73-0 76-16-4 2551-62-4
(***plasma*** ***etching*** by oxygen and, of silicon, mechanism of)
IT 7440-21-3, reactions
(***plasma*** ***etching*** of, mechanism of, cantilever structures in)

L40 ANSWER 23 OF 23 HCA COPYRIGHT 1999 ACS
93:177188 Perforated screen for an electron beam irradiation device. Wada, Hirotsugu; Shinozaki, Toshiaki (VLSI Technology Research Association, Japan). Ger. Offen. DE 2944576 19800508, 15 pp. (German). CODEN: GWXXBX. PRIORITY: JP 78-136483 19781106.
AB A process for the prepn. of a perforated screen involves forming projecting segments on one side of a substrate by ***etching*** , filling the ***etched*** indentations around these segments with a screen material, and then removing the substrate. Thus, a Si single-crystal platelet with [100] surface was thermally ***oxidized*** on both sides, on one side a ***resist*** or ***photoresist*** pattern was applied, the SiO2 was selectively ***etched*** , and then the Si platelet with the unetched ***SiO2*** as ***mask*** was ***anisotropically*** ***etched*** with aq. KOH and iso-PrOH at 60.degree. to leave a rectangular pattern with rectangular-trapezoidal vertical cross sections whose lateral surfaces are formed from the [111] surface of Si. On the upper side of the exposed Si an elec. conducting screening material such as Au, Ag, or Cu was applied by electroplating and the remaining SiO2 was removed by means of an NH4F soln. Then the Si substrate was removed by ***plasma*** ***etching*** or alk. soln. to leave a perforated screen having holes of very high measurement precision suitable for use in an electron beam app.or the like.
IC C25D001-02; C23F001-02; G02B005-00
CC 74-1 (Radiation Chemistry, Photochemistry, and Photographic Processes)
Section cross-reference(s): 71, ***76***
IT 7440-21-3, uses and miscellaneous
(electrodeposition of metallic screening material on ***silica*** - ***masked*** , in prepn. of perforated screens for electron beam irradn. devices)

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L41 ANSWER 1 OF 5 HCA COPYRIGHT 1999 ACS
123:354458 Applications of ***plasma*** polymerized methylsilane as a resist and silicon dioxide precursor for 193 and 248 nm lithography. Weidman, T. W.; Joubert, O.; Joshi, A. M.; Kostelak, R. L. (ATandT Bell Laboratories, Murray Hill, NJ, 07974, USA). Proc. SPIE-Int. Soc. Opt. Eng., 2438(Advances in Resist Technology and Processing XII), 496-503 (English) 1995. CODEN: PSISDG. ISSN: 0277-786X.
AB Silicon dioxide is the primary ***dielec*** . fabric of silicon integrated circuits, and the need to pattern it accounts for a large percentage of all photolithog. operations. As shrinking device dimensions place extreme demands on both lithog. and ***etching*** , patterned oxide films are finding yet addnl. applications as intermediate " ***hard*** ***masks*** ". For example, polysilicon gate and metal layers may be ***etched*** with greater selectivity and linewidth control through a thin patterned oxide mask, rather than through a thicker photoresist layer (which is used to pattern the oxide and removed before pattern transfer).

However, any advantages of such schemes must be weighed against the costs of increasing process complexity. We recently reported a new all-dry photolithog. process based on the ***plasma*** deposition and patterning of organosilicon resists. These materials, as best exemplified by ***plasma*** polymd. methylsilane (PPMS), possess amorphous Si-Si bond backbone structures and undergo efficient photo- ***oxidn*** . to give glass-like siloxane network material. Patterns are developed using chlorine ***plasma*** ***etching*** to selectively remove unexposed regions, providing a neg. tone image. In previous papers we have demonstrated the use of these materials in bilevel processes, using oxygen reactive ion ***etching*** to transfer patterns in thin PPMS layers through underlying org. planarizing layers. Using 248 nm deep UV exposure tools, such schemes afford sub-0.25 .mu.m design rule capabilities and are well suited for difficult device topog. Here we describe the discovery and development of a fundamentally different application unique to PPMS: a new direct approach to patterned silicon dioxide.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

IT ***Oxidation*** , photochemical
Photomasks
(***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT Siloxanes and Silicones, uses
(***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT Sputtering
(***etching*** , ***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT Electric circuits
(integrated, ***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT Lithography
Resists
(photo-, ***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT ***Etching***
(sputter, ***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT 110477-49-1P, Poly(methylsilane)
(***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

IT 992-94-9, Methylsilane
(***plasma*** polymd. methylsilane as resist and silicon dioxide precursor for photolithog.)

L41 ANSWER 2 OF 5 HCA COPYRIGHT 1999 ACS

122:42547 A comparison of dry ***etch*** approaches for tungsten ***patterning*** . Dobisz, Elizabeth A.; Eddy, Charles, Jr.; Kosakowski, John; Glembocki, Orest J.; Shirey, Loretta M.; Foster, Kelly W.; Chu, William; Rhee, Kee Woo; Park, Doewan; et al. (Naval Research Laboratory, Washington, DC, 20375, USA). Proc. SPIE-Int. Soc. Opt. Eng., 2194(Electron-Beam, X-Ray, and Ion-Beam Submicrometer Lithographies for Manufacturing IV), 178-86 (English) 1994. CODEN: PSISDG. ISSN: 0277-786X.

AB The results of the NRL program focusing on high resoln., high aspect ratio, ***patterning*** of W is summarized. The work investigates three parallel approaches: reactive ion ***etching*** (RIE), electron cyclotron resonance (ECR) ***etching*** , and

chem. assisted ion beam ***etching*** (CAIBE). Key issues that are analyzed for each process are the ***etch*** ***mask*** , anisotropy, selectivity, ***etch*** ***stop*** , compatibility with high resoln. (sub-250 nm) lithog. ***patterning*** of W, and applicability to membranes. In the first two methods, prevention of sidewall undercutting is the key issue. Here the effort focuses on sidewall passivation and substrate cooling. RIE is a commonly utilized fabrication tool and the process has been developed to ***etch*** 100 nm lines. ECR is a relatively new process and it has more degrees of freedom than RIE. For example, the magnetic field configuration has been modeled to characterize the ***plasma*** position and the magnet configuration has been optimized. Both SF6 chem. and CBrF3 chem. have been investigated. In the case of CAIBE, no undercutting was obsd., but ***mask*** erosion was apparent in many cases. Methods to minimize the ***mask*** erosion are described and a comparison of Cl2 chem. to SF6 chem. is made. The results on the three dry ***etching*** techniques will be described and contrasted.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

ST tungsten ***plasma*** ***etching*** lithog ***mask*** ; reactive ion ***etching*** tungsten lithog ***mask*** ; electron cyclotron resonance ***etching*** tungsten; chem assisted ion beam ***etching*** tungsten; x ray lithog ***mask*** tungsten ***etching***

IT ***Etching***
(electron cyclotron resonance; comparison of dry ***etch*** approaches of tungsten ***patterning*** for x-ray lithog. ***mask*** fabrication)

IT Sputtering
(***etching*** , ion-beam, reactive, comparison of dry ***etch*** approaches of tungsten ***patterning*** for x-ray lithog. ***mask*** fabrication)

IT Sputtering
(***etching*** , reactive, comparison of dry ***etch*** approaches of tungsten ***patterning*** for x-ray lithog. ***mask*** fabrication)

IT ***Etching***
(sputter, ion-beam, reactive, comparison of dry ***etch*** approaches of tungsten ***patterning*** for x-ray lithog. ***mask*** fabrication)

IT ***Etching***
(sputter, reactive, comparison of dry ***etch*** approaches of tungsten ***patterning*** for x-ray lithog. ***mask*** fabrication)

IT ***Photomasks***
(x-ray, comparison of tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance and chem. assisted ion beam ***etching*** for)

IT 7440-33-7, Tungsten, processes
(comparison of tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance and chem. assisted ion beam ***etching*** for x-ray lithog. ***mask*** fabrication)

IT 7440-47-3, Chromium, processes
(***etch*** - ***stop*** ***mask*** ; comparison of tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance and chem. assisted ion beam ***etching*** for x-ray lithog. ***mask*** fabrication)

IT 2551-62-4, Sulfur hexafluoride
(***plasma*** contg.; comparison of tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance and chem. assisted ion beam ***etching*** for lithog. x-ray ***masks*** fabrication)
IT 7782-50-5, Chlorine, processes 14791-69-6, Argon(1+), processes
(***plasma*** contg.; tungsten ***patterning*** by chem. assisted ion beam ***etching*** for x-ray lithog. ***mask*** fabrication)
IT 75-63-8, Trifluorobromomethane 7440-37-1, Argon, processes
(***plasma*** contg.; tungsten ***patterning*** by electron cyclotron resonance ***etching*** for x-ray lithog. ***mask*** fabrication)
IT ***7782-44-7*** , Oxygen, processes
(***plasma*** contg.; tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance ***etching*** for x-ray lithog. ***mask*** fabrication)
IT 75-46-7, Trifluoromethane 1333-74-0, Hydrogen, processes 7440-59-7, Helium, processes 7727-37-9, Nitrogen, processes
(***plasma*** contg.; tungsten ***patterning*** by reactive ion ***etching*** for x-ray lithog. ***mask*** fabrication)
IT 9011-14-7, PMMA 119574-53-7, SAL-601
(***resist*** ; comparison of tungsten ***patterning*** by reactive ion ***etching*** and electron cyclotron resonance and chem. assisted ion beam ***etching*** for x-ray lithog. ***mask*** fabrication)

L41 ANSWER 3 OF 5 HCA COPYRIGHT 1999 ACS
122:42546 Reactive ion ***etching*** of tungsten for high resolution x-ray ***masks*** . Shirey, Loretta M.; Foster, Kelly W.; Chu, William; Kosakowski, John; Rhee, Kee Woo; Dobisz, Elizabeth A.; Eddy, Charles Jr.; Park, Doewon; Isaacson, I. Peter; et al. (Nanoelectronics Processing Facility, Naval Research Laboratory, Washington, DC, 20375, USA). Proc. SPIE-Int. Soc. Opt. Eng., 2194(Electron-Beam, X-Ray, and Ion-Beam Submicrometer Lithographies for Manufacturing IV), 169-77 (English) 1994. CODEN: PSISDG. ISSN: 0277-786X.
AB A process for ***etching*** fine features in tungsten (100nm linewidth or less) to produce ***patterned*** absorbers has been developed. The ***pattern*** is first defined in a chrome ***etch*** ***mask*** on the tungsten absorber layer using e-beam lithog. and is then transferred into the tungsten by Reactive-Ion- ***Etching*** . H2 is mixed with SF6 to passivate the sidewalls of the tungsten features because SF6 alone causes severe undercutting of the features. Control of undercutting is the key challenge in reactive ion ***etching*** of tungsten. With an optimum mixt. of 20% H2 and 80% SF6, plus substrate cooling to -25.degree.C, undercutting can be controlled for 250nm geometries. Increased undercutting has been obsd. at the endpoint of the ***etching*** process, the chromium ***etch*** ***stop*** layer. In this case the fluorine radical concn. increases as a result of the diminished amt. of tungsten, thereby promoting ***etching*** of the sidewalls. This mechanism is demonstrated through a computer model. The endpoint can be controlled through laser endpoint detection. For sub 250nm geometries, addnl. sidewall passivation is accomplished with an intermittent ***etch*** process, thereby allowing the ***etching*** of high aspect ratio 100nm features in 650nm thick tungsten layers.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and

Other Reprographic Processes)
ST tungsten ***etching*** x ray ***mask*** lithog; reactive ion ***etching*** tungsten microlithog
IT Sputtering
(***etching*** , reactive, reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT ***Etching***
(sputter, reactive, reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT ***Photomasks***
(x-ray, reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT 7440-47-3, Chromium, processes
(***etch*** ***stop*** layer; reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT 75-46-7, Trifluoromethane 1333-74-0, Hydrogen, processes 2551-62-4, Sulfur hexafluoride 7440-59-7, Helium, processes 7727-37-9, Nitrogen, processes ***7782-44-7*** , Oxygen, processes
(***plasma*** ; reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT 7440-33-7, Tungsten, processes
(reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)
IT 9011-14-7, PMMA
(***resist*** ; reactive ion ***etching*** of tungsten for high resoln. x-ray ***masks***)

L41 ANSWER 4 OF 5 HCA COPYRIGHT 1999 ACS
117:100781 Novel resist patterning strategies for the definition of high resolution via holes in polyimide inter-layer ***dielectric*** . Martin, Brian; Harper, Neil (GEC Plessey Semicond., Roborough/Plymouth/Devon, PL6 7BQ, UK). Proc. SPIE-Int. Soc. Opt. Eng., 1672(Adv. Resist Technol. Process. IX), 586-96 (English) 1992. CODEN: PSISDG. ISSN: 0277-786X.
AB Lithog. for via holes in polyimide is conventionally restricted by the need for a thick masking resist due to poor ***plasma*** selectivity during pattern transfer. Two novel techniques for via hole definition are described. The 1st is a single-layer masking process using a Si-contg. resist, which presents high resistance to O ***plasma*** , while the other is a ***hard*** ***masking*** process using spin-on-glass. Processing and characterization for each technique is described and compared with the std. process.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
ST resist patterning via hole polyimide ***dielec*** ; lithog ***etching*** via hole polyimide silicon; spin on glass mask resist pattern
IT ***Etching***
(resist patterning strategies in, for definition of high resoln. via holes)
IT 75-46-7, Trifluoromethane
(dry ***etching*** of spin-on-glass using mixt. of oxygen and, resist patterning strategies for high resoln. via holes in relation to)
IT ***7782-44-7*** , Oxygen, properties
(reactive ion ***etching*** using, pattern transfer into polyimides by, resist patterning strategies for)

L41 ANSWER 5 OF 5 HCA COPYRIGHT 1999 ACS
116:72075 Tungsten ***patterning*** for 1:1 x-ray ***masks*** .
Jurgensen, C. W.; Kola, R. R.; Novembre, A. E.; Tai, W. W.;
Frackoviak, J.; Trimble, L. E.; Celler, G. K. (AT and T Bell Lab.,
Murray Hill, NJ, 07974, USA). J. Vac. Sci. Technol., B, 9(6),
3280-6 (English) 1991. CODEN: JVTBD9. ISSN: 0734-211X.
AB A subtractive process to form subhalf micron, vertical-walled ***patterns*** in half-micron thick tungsten on x-ray ***masks*** was developed. Electron-beam lithog. was used to form ***resist*** ***patterns*** on a structure consisting of 300 .ANG. Cr on 5000 .ANG. W on 200 .ANG. Cr on an ~1 .mu.m thick poly-silicon or silicon nitride membrane. The Cr ***masking*** and ***etch*** - ***stop*** layers above and below the W layer are required because the ***resist*** and membrane materials ***etch*** rapidly in fluorine based W ***etching*** ***plasmas*** . Chromium was chosen for these layers because it has a high selectivity in the W ***etch*** (.apprxeq.40:1), is compatible with the W deposition process, and can be ***patterned*** in an ***O2*** -Cl2 ***plasma*** which does not ***etch*** W or the membrane materials. Helium backside cooling at a pressure 1-5 torr controls membrane temp. during all ***plasma*** processing steps. Pure CBrF3 or CHF3 ***etch*** W slowly while simultaneously depositing polymer which produces sloping profiles where the base of the feature is wider than the initial ***mask*** width. Pure SF6 gives high ***etching*** rates but the fluorine radicals attack the W sidewall causing undercutting. Depositing polymer on the sidewall by adding CHF3 or CBrF3 to the SF6 reduces undercutting, but produces sloping profiles. The undercutting found with pure SF6 can be eliminated with vertical profiles by ***etching*** at low temp. or by adding N2 or Cl2 to the gas mixt. to form low volatility reaction products with tungsten on the sidewall.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
ST tungsten ***patterning*** x ray ***mask***
IT Lithography
(electron-beam, in tungsten ***patterning*** for subhalf-micron lithog. x-ray ***mask*** fabrication)
IT ***Photomasks***
(x-ray, tungsten ***patterning*** for, for subhalf-micron lithog.)
IT 7440-21-3, Silicon, uses 7440-47-3, Chromium, uses
(in fabrication of x-ray ***masks*** with tungsten absorber for subhalf-micron lithog.)
IT 7440-33-7, Tungsten, uses
(***patterning*** of, in x-ray ***mask*** fabrication for sub-half-micron lithog.)
IT 75-46-7, Trifluoromethane 75-63-8, Bromotrifluoromethane
2551-62-4, Sulfur hexafluoride 7727-37-9, Nitrogen, uses
7782-44-7 , Oxygen, uses 7782-50-5, Chlorine, uses
(***plasma*** contg., in tungsten ***patterning*** for x-ray ***masks*** for subhalf-micron lithog.)

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L42 ANSWER 1 OF 28 HCA COPYRIGHT 1999 ACS
130:132683 Integration of SAC and SALICIDE processes on a chip having
embedded memory. Huang, Jenn Ming (Taiwan Semiconductor
Manufacturing Company, Ltd., Taiwan). U.S. US 5863820 A 19990126,

12 pp. (English). CODEN: USXXAM. APPLICATION: US 98-17480
19980202.

AB A process and structure are described in which logic and memory share the same chip. Contacts to the memory circuits are made using the SAC (self-aligned contact) process, thus ensuring max. d., while the logic circuits are made using the SALICIDE (self-aligned silicide) process, thus ensuring high performance. The 2 processes have been integrated within a single chip by 1st forming polysilicon gate pedestals, those located in the memory areas also having ***hard*** ***masks*** of Si nitride. Next, spacers are grown on the vertical sides of the pedestals. Source/drain regions are now formed using the LDD process, following which the pedestals, on the memory side only, are given a protective coating of oxide. This allows the SALICIDE process to be selectively applied to only the logic side. Then, while the logic side is protected, the SAC process is applied to the memory side. This process is self-aligning. The spacers define the contact holes and the ***hard*** ***masks*** allow oversize openings to be ***etched*** without the danger of shorting through to the pedestals.

IC ICM H01L021-8242
ICS H01L021-3205; H01L021-4763

NCL 438241000

CC ***76-3*** (Electric Phenomena)

ST integration SAC SALICIDE process logic memory circuit; polysilicon gate pedestal logic memory circuit; silicon nitride ***hard*** ***mask*** logic memory circuit; self aligned contact silicide logic memory circuit

IT ***Photomasks*** (lithographic ***masks***)
(***hard*** ; integration of SAC and SALICIDE processes on a chip having logic and memory devices using silicon nitride ***hard*** ***masks***)

IT ***Photoresists***
Plasma ***etching***
(in integration of SAC and SALICIDE processes on a chip having logic and memory devices)

IT Coatings
(protective oxide coatings; in integration of SAC and SALICIDE processes on a chip having logic and memory devices using silicon nitride ***hard*** ***masks***)

IT 7727-37-9, Nitrogen, processes ***7782-44-7*** , Oxygen, processes
(***etching*** by ***O2*** /N2 ***plasma*** ; in integration of SAC and SALICIDE processes on a chip having logic and memory devices)

IT 7782-41-4, Fluorine, processes
(***etching*** by; in integration of SAC and SALICIDE processes on a chip having logic and memory devices)

IT 12033-89-5, Silicon nitride, processes
(integration of SAC and SALICIDE processes on a chip having logic and memory devices using silicon nitride ***hard*** ***masks***)

L42 ANSWER 2 OF 28 HCA COPYRIGHT 1999 ACS

130:46049 Reduction of ***plasma*** process-induced damage during gate poly ***etching*** by using a SiO2 ***hard*** ***mask*** . Lee, H. C.; Creusen, M.; Groeseneken, G.; Vanhaelemeersch, S. (IMEC vzw, Louvain, 3001, Belg.). Int. Symp. Plasma Process-Induced Damage, 3rd, 72-75. Editor(s): Nakamura, Moritaka; Dao, Thuy; Hook, Terence. Northern California Chapter of

the American Vacuum Society: Sunnyvale, Calif. (English) 1998.
CODEN: 66XPA6.

AB The redn. was studied of elec. and phys. ***plasma*** damage by replacing a ***photoresist*** mask with a silica mask for gate polysilicon ***patterning*** . Significant redn. is obsd. Using HBr/ ***O2*** chem. reduces phys. damage even more. Selective ***oxidn*** . of polysilicon is increased. These results appear to be due to the absence of carbon impurities derived from the ***photoresist*** .

CC ***76-11*** (Electric Phenomena)

ST silica mask ***plasma*** ***etching*** polysilicon

IT ***Etching*** masks
Photoresists
Plasma ***etching***
Polycrystalline materials
(redn. of elec. and phys. ***plasma*** damage by replacing ***photoresist*** mask with silica mask for gate polysilicon ***patterning***)

IT Selective ***oxidation***
(redn. of elec. and phys. ***plasma*** damage by replacing ***photoresist*** mask with silica mask for gate polysilicon ***patterning*** and)

IT 7440-21-3, Silicon, processes
(redn. of elec. and phys. ***plasma*** damage by replacing ***photoresist*** mask with silica mask for gate polysilicon ***patterning***)

IT ***7782-44-7*** , Oxygen, reactions 10035-10-6, Hydrogen bromide, reactions
(redn. of elec. and phys. ***plasma*** damage by replacing ***photoresist*** mask with silica mask for gate polysilicon ***patterning***)

IT 7631-86-9, Silica, uses
(redn. of elec. and phys. ***plasma*** damage by replacing ***photoresist*** mask with silica mask for gate polysilicon ***patterning***)

L42 ANSWER 3 OF 28 HCA COPYRIGHT 1999 ACS

129:297082 Shallow trench ***etch*** with a planar inductively coupled ***plasma*** discharge. Yu, Bo; Zhong, Qinghua; Zhou, Meisheng (Institute of Microelectronics, Singapore, 117685, Singapore). Proc. - Electrochem. Soc., 98-4(Plasma Processing), 222-230 (English) 1998. CODEN: PESODO. ISSN: 0161-6374. Publisher: Electrochemical Society.

AB The shallow Si trench ***etching*** for shallow trench isolation was studied using a planar inductively coupled ***plasma*** discharge chamber with different chemistries and ***etch*** mask. Both HBr/Cl2/ ***O2*** and Cl2/ ***O2*** chemistries with nitride ***hard*** ***mask*** demonstrated the process capability in terms of ***etch*** nonuniformity, ***etch*** rate, depth microloading, profile microloading effect, profile angle control. Also the ***O2*** flow is the key factor to achieve sloped trench profile, and the pressure and source power are the parameters to tune the nonuniformity and improve bottom corner rounding. Compared with ***photoresist*** mask, the trench ***etching*** with Si3N4 as ***hard*** ***mask*** showed better profile, profile angle variation and ***etch*** rate nonuniformity.

CC ***76-11*** (Electric Phenomena)

ST shallow trench ***plasma*** ***etching*** silicon

IT ***Etching*** masks

Flow
  Photoresists
  Plasma ***etching***
  Plasma ***etching*** kinetics
Semiconductor device fabrication
   (shallow trench ***etching*** of silicon with planar
   inductively coupled ***plasma*** discharge)

IT 7440-21-3, Silicon, processes 7631-86-9, Silica, processes
12033-89-5, Silicon nitride (Si3N4), processes
   (shallow trench ***etching*** of silicon with planar
   inductively coupled ***plasma*** discharge)

IT 75-73-0, Tetrafluoromethane 2551-62-4, Sulfur hexafluoride
7782-44-7 , Oxygen, reactions 7782-50-5, Chlorine,
reactions 10035-10-6, Hydrogen bromide, reactions
   (shallow trench ***etching*** of silicon with planar
   inductively coupled ***plasma*** discharge)

L42 ANSWER 4 OF 28 HCA COPYRIGHT 1999 ACS

129:209234 Low-stress sputtered chromium-nitride ***hard*** - ***masks*** and their ***etching*** characteristics for X-ray mask fabrication. Tsuboi, Shinji; Seki, Miyoshi; Kotsuji, Setsu; Yoshihara, Takuya; Fujii, Kiyoshi; Suzuki, Katsumi (Silicon Systems Research Laboratories, NEC Corp., Japan). NEC Res. Dev., 39(2), 127-133 (English) 1998. CODEN: NECRAU. ISSN: 0547-051X. Publisher: NEC Culture Center, Ltd..

AB Fabrication of precise x-ray masks is 1 of the most important issues in synchrotron radiation (SR) lithog. To achieve high-precision x-ray masks, the authors have developed a low-stress Cr-Nitride (CrN) ***hard*** - ***mask*** . Both the stress and its distribution (gradient) in the CrN films, which are elec. conductive, are within measurement error. Using a 75. nm-thick CrN ***hard*** - ***mask*** , 0.10 .mu.m line-and-space ***patterns*** in a 0.4 .mu.m-thick Ta-Ge (TaGe) alloy x-ray absorber were demonstrated. The CrN film was ***etched*** by reactive-ion ***etching*** using Cl ***gas*** mixed with ***O*** . The ***etching*** selectivity between the TaGe alloy and the CrN was 13 when using Electron-Cyclotron-Resonance (ECR) ***plasma*** ***etching*** with S hexafluoride gas. The authors have also studied the durability of CrN to various acids; e.g., APM (NH3:H2O2:H2O), HPM (HCl:H2O2:H2O), and SPM (H2SO4:H2O2); widely used in Si-wafer cleaning processes. The CrN ***etching*** rate for those acids was <3 nm/min. A sputtered CrN film is an excellent ***hard*** - ***mask*** material for precise x-ray mask fabrication.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): ***76***

ST sputtered chromium nitride ***hard*** ***mask*** ***etching*** ; chromium nitride x ray mask fabrication

IT Electric conductivity
  Etching kinetics
Photomasks (lithographic masks)
  Plasma
Radio frequency sputtering
Reactive ion ***etching***
X-ray masks
   (low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)

IT ***Photoresists***

(neg. e-beam; low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)
IT Lithography
(synchrotron-radiation; low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)
IT 12705-37-2, Chromium-nitride
(low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)
IT 2551-62-4, Sulfur fluoride (SF6) 7647-01-0, Hydrochloric acid, reactions 7664-39-3, Hydrofluoric acid, reactions 7664-41-7, Ammonia, reactions 7664-93-9, Sulfuric acid, reactions 7722-84-1, Hydrogen peroxide, reactions 7732-18-5, Water, reactions
(low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)
IT 57854-33-8
(low-stress sputtered chromium-nitride ***hard*** - ***masks*** and ***etching*** characteristics for x-ray mask fabrication)

L42 ANSWER 5 OF 28 HCA COPYRIGHT 1999 ACS
129:168006 ***Pattern*** ***etching*** of Ta x-ray mask absorber on SiC membrane by inductively coupled ***plasma*** . Iba, Yoshihisa; Kumasaka, Fumiaki; Aoyama, Hajime; Taguchi, Takao; Yamabe, Masaki (Fujitsu Laboratories Ltd., Morinosato-Wakaniya, Atsugi, 243-0197, Japan). Jpn. J. Appl. Phys., Part 2, 37(7A), L824-L826 (English) 1998. CODEN: JAPLD8. ISSN: 0021-4922. Publisher: Japanese Journal of Applied Physics.
AB ***Patterning*** of an x-ray mask absorber after Si back- ***etching*** is desirable from the viewpoint of the ***pattern*** placement accuracy. We investigated Ta x-ray absorber ***etching*** on an SiC membrane equipped on a mask frame using a low-stress CrN ***hard*** ***mask*** and an ICP ***etcher*** with a He cooling system. In this system, the membrane temp. and the self-bias voltage could be controlled. A 40-nm-thick CrN film was ***etched*** using a 200-nm-thick ***resist*** and Cl2 and ***O2*** gases with a selectivity of 0.72 and a vertical sidewall. A 400-nm-thick Ta film was ***etched*** using Cl2 gas at an electrode temp. of -10.degree. and a low gas pressure of 0.1 Pa. A high selectivity of Ta to CrN, 42, was obtained, and lines and spaces ***patterns*** below 0.1 .mu.m with vertical sidewalls could be fabricated.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): ***76***
ST ***etching*** tantalum x ray mask absorber; silicon carbide membrane x ray mask
IT ***Plasma*** ***etching***
X-ray masks
(***pattern*** ***etching*** of Ta x-ray mask absorber on SiC membrane by inductively coupled ***plasma***)
IT 409-21-2, Silicon carbide (SiC), uses 7440-25-7, Tantalum, uses 24094-93-7, Chromium nitride (CrN)
(***pattern*** ***etching*** of Ta x-ray mask absorber on SiC membrane by inductively coupled ***plasma***)
IT ***7782-44-7*** , Oxygen, uses 7782-50-5, Chlorine, uses

(***pattern*** ***etching*** of Ta x-ray mask absorber on SiC membrane by inductively coupled ***plasma***)

L42 ANSWER 6 OF 28 HCA COPYRIGHT 1999 ACS
129:11379 Iron nitride mask and reactive ion ***etching*** of GaN films. Lee, Heon; Harris, James S., Jr. (Solid State Electronics Lab., Stanford Univ., Stanford, CA, 94305, USA). J. Electron. Mater., 27(4), 185-189 (English) 1998. CODEN: JECMA5. ISSN: 0361-5235. Publisher: Minerals, Metals & Materials Society.

AB One of the major GaN processing challenges is useful ***pattern*** transfer. Serious ***photoresist*** ***mask*** erosion and ***hardening*** are often obsd. in reactive ion ***etching*** of GaN. Fine ***pattern*** transfer to GaN films using ***photoresist*** masks and complete removal of remaining ***photoresist*** after ***etching*** are very difficult. By replacing the ***etch*** mask from conventional ***photoresist*** to a sputtered iron nitride (Fe-8% N) film, which is easily ***patterned*** by wet chem. ***etching*** and is very resistive to Cl based ***plasmas*** , GaN films can be finely ***patterned*** with vertical ***etched*** sidewalls. Successful ***pattern*** transfer is realized by reactive ion ***etching*** using Cl (H) contg. ***plasmas*** . CHF3/Ar, C2ClF5/Ar, C2ClF5/Ar/ ***O2*** , SiCl4, and CHCl3 ***plasmas*** were used to ***etch*** GaN. The GaN ***etch*** rate is dependent on the cryst. quality of GaN. Higher cryst. quality GaN films exhibit slower ***etch*** rates than GaN films with higher dislocation and stacking fault d.

CC ***76-3*** (Electric Phenomena)

ST gallium nitride reactive ion ***etching*** mask; iron nitride mask reactive ion ***etching***

IT ***Etching*** masks
(iron nitride mask and reactive ion ***etching*** of GaN films)

IT ***Photoresists***
(mask; iron nitride mask and reactive ion ***etching*** of GaN films)

IT Reactive ion ***etching***
(of gallium nitride film; iron nitride mask and reactive ion ***etching*** of GaN films)

IT Crystal dislocations
Crystallinity
(of gallium nitride; iron nitride mask and reactive ion ***etching*** of GaN films)

IT Erosion (wear)
Hardening (mechanical)
(of ***mask*** ; iron nitride mask and reactive ion ***etching*** of GaN films)

IT Transfers
(***pattern*** ; iron nitride mask and reactive ion ***etching*** of GaN films)

IT 37245-77-5, Iron nitride
(***etching*** mask; iron nitride mask and reactive ion ***etching*** of GaN films)

IT 207510-37-0, Iron 92, nitrogen 8
(***etching*** mask; iron nitride mask and reactive ion ***etching*** of GaN films)

IT 10026-04-7, Silicon chloride (SiCl4)
(iron nitride mask and reactive ion ***etching*** of GaN films)

IT 75-46-7, Fluoroform 76-15-3 354-56-3 7440-37-1, Argon,

properties ***7782-44-7*** , Oxygen, properties
(of gallium nitride; iron nitride mask and reactive ion ***etching*** of GaN films)

IT 25617-97-4, Gallium nitride (GaN)
(reactive ion ***etching*** of; iron nitride mask and reactive ion ***etching*** of GaN films)

L42 ANSWER 7 OF 28 HCA COPYRIGHT 1999 ACS

128:316144 Fabrication of semiconductor device. Akahori, Takashi; Ishizuka, Shuichi; Endo, Shunichi; Aoki, Takeshi; Hirata, Tadashi (Tokyo Electron Ltd., Japan; Akahori, Takashi; Ishizuka, Shuichi; Endo, Shunichi; Aoki, Takeshi; Hirata, Tadashi). PCT Int. Appl. WO 9821745 A1 19980522, 26 pp. DESIGNATED STATES: W: KR, US; RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (Japanese). CODEN: PIXXD2. APPLICATION: WO 97-JP4099 19971111. PRIORITY: JP 96-320912 19961114.

AB A process for the prodn. of a semiconductor device is described, which enables the practical use of a F-contg. C film (hereinafter referred to as a CF film) as the interlayer insulator film. The deposition of a conductive film such as a TiN film on a CF film and the patternwise deposition of a ***resist*** film on the film are conducted successively, followed by ***etching*** of the TiN film. Although the subsequent irradn. of the resulting wafer with an ***O2*** ***plasma*** ***etches*** not only the CF film but also the ***resist*** film, predetd. holes can be formed by virtue of the action of the TiN film as a mask. Then, wiring is formed of Al or the like on the surface of the CF film. The TiN film is effective in making the wiring and the CF film adhere tightly to each other and serves as a part of the wiring. An insulator film made of SiO2 or the like may be used as the mask instead of the conductive film.

IC ICM H01L021-3065

CC ***76-3*** (Electric Phenomena)

ST semiconductor device fluorine carbon insulator film; ***etching*** fluorine carbon insulator film semiconductor

IT Interconnections (electric)
(***etching*** of F-contg. carbon insulator film for)

IT Semiconductor device fabrication
(***etching*** of F-contg. carbon insulator film in)

IT ***Dielectric*** films
(***etching*** of F-contg. carbon insulator film in semiconductor device fabrication)

IT ***Etching*** masks
(in ***etching*** of F-contg. carbon insulator film in semiconductor device fabrication)

IT ***Plasma*** ***etching***
(of F-contg. carbon insulator film in semiconductor device fabrication)

IT 7440-44-0, Carbon, processes 7782-41-4, Fluorine, processes
(***etching*** of F-contg. carbon insulator film in semiconductor device fabrication)

IT ***7631-86-9*** , ***Silica*** , processes 25583-20-4, Titanium ***nitride*** (TiN)
(***mask*** ; in ***etching*** of F-contg. carbon insulator film in semiconductor device fabrication)

IT ***7782-44-7*** , Oxygen, processes
(***plasma*** ; ***etching*** of F-contg. carbon insulator film in semiconductor device fabrication)

IT 7429-90-5, Aluminum, processes
(wiring; ***etching*** of F-contg. carbon insulator film for)

L42 ANSWER 8 OF 28 HCA COPYRIGHT 1999 ACS
128:302945 Method for making planar metal interconnections and metal plugs on semiconductor substrates. Tseng, Horng-huei (Vanguard International Semiconductor Corp., Taiwan). U.S. US 5741741 A 19980421, 11 pp. (English). CODEN: USXXAM. APPLICATION: US 96-652175 19960523.

AB A method for making planar metal interconnections and T-shaped metal plugs for integrated circuits is achieved. The method involves forming a planar insulating SiO2 film and a ***hard*** ***mask*** film over a 1st level of interconnections. A ***patterned*** 1st ***photoresist*** layer is then formed for ***etching*** trenches in the ***hard*** ***mask*** film and partially into the planar insulating layer in which a 2nd level of interconnections are to be formed. The ***patterned*** ***photoresist*** layer is then laterally ***etched*** to expose the ***hard*** ***mask*** adjacent to the trenches in the SiO2, and the ***hard*** ***mask*** is then removed adjacent to the trenches to form a self-aligned mask for the metal plug contact openings. A ***patterned*** 2nd ***photoresist*** mask aligned over the trenches is then used to ***etch*** the contact openings in the trenches, using the ***hard*** ***mask*** to form T-shaped plug contact openings to the 1st level of interconnections. The trenches and plug contact openings are concurrently filled with CVD Al and chem.-mech. polished back to form the 2nd level of interconnections with T-shaped metal plugs. The T-shaped metal plugs improve the edge coverage while making it easier to fill the narrow contact openings with Al without voids in the metal plugs.

IC ICM H01L021-44

NCL 438637000

CC ***76-2*** (Electric Phenomena)

IT Contact holes
(***etching*** of; in making planar metal interconnections and metal plugs on semiconductor substrates)

IT Photomasks (lithographic masks)
Photoresists
Plasma ***etching***
(in making planar metal interconnections and metal plugs on semiconductor substrates)

IT ***7782-44-7*** , Oxygen, processes
(***plasma*** ***etching*** by; in making planar metal interconnections and metal plugs on semiconductor substrates)

L42 ANSWER 9 OF 28 HCA COPYRIGHT 1999 ACS
128:224630 Problems and solutions for low pressure, high density, inductively coupled ***plasma*** dry ***etch*** applications. Puttock, Mark (Littleton Upon Severn, Electrotech Ltd, Bristol, BS12 1NP, UK). Surf. Coat. Technol., 97(1-3), 10-14 (English) 1997. CODEN: SCTEEJ. ISSN: 0257-8972. Publisher: Elsevier Science S.A..

AB Dry ***etching*** for mainstream microelectronics applications has undergone a shift in the past few years towards high d. ***plasma*** reactor designs. Such sources operate at lower pressure which helps avoid undercutting when ***etching*** small features (<0.6 .mu.m), however, new problems also arise, and in this paper a selection of these is aired. Results from the Electrotech Omega 201 inductively coupled ***plasma*** ***etcher*** are used to reach the following conclusions: for prodn. aluminum alloy ***etching*** , selectivity to ***photoresist*** can be

significantly improved by use of HBr chem.; for prodn. dry develop of ***photoresist*** , an SO2- ***O2*** mixt. can be used to give zero CD loss; and for copper ***etching*** , residue-free results are achieved on test wafers at a temp. of >240 .degree.C.
CC ***76-11*** (Electric Phenomena)
Section cross-reference(s): 56, 74
ST ICP dry ***etching*** microelectronics; aluminum alloy interconnect ICP dry ***etching*** ; ***photoresist*** dry develop cd loss; copper dry ***etching*** ***hard*** ***mask*** ICP
IT Interconnections (electric)
(Al alloy; problems and solns. for low pressure, high d., inductively coupled ***plasma*** dry ***etch*** applications for)
IT ***Photoresists***
(cd loss in dry develop prodn. of)
IT Dry ***etching***
Inductively coupled ***plasma***
(problems and solns. for low pressure, high d., inductively coupled ***plasma*** dry ***etch*** applications)
IT Microelectronics
(problems and solns. for low pressure, high d., inductively coupled ***plasma*** dry ***etch*** applications for)
IT Circular dichroism
(zero loss; cd loss in dry develop prodn. of ***photoresists***)
IT aluminum alloy, base
(interconnects; problems and solns. for low pressure, high d., inductively coupled ***plasma*** dry ***etch*** applications for)
IT 7440-50-8, Copper, processes
(***hard*** ***mask*** dry ***etching*** ; problems and solns. for low pressure, high d., inductively coupled ***plasma*** dry ***etch*** applications for)

L42 ANSWER 10 OF 28 HCA COPYRIGHT 1999 ACS
127:255944 Low-k fluorinated amorphous carbon interlayer technology for quarter micron devices. Matsubara, Y.; Endo, K.; Tatsumi, T.; Ueno, H.; Sugai, K.; Horiuchi, T. (ULSI Device Development Labs., NEC Corp., Kanagawa, 229, Japan). Tech. Dig. - Int. Electron Devices Meet. 369-372 (English) 1996. CODEN: TDIMD5. ISSN: 0163-1918. Publisher: Institute of Electrical and Electronics Engineers.
AB The authors have developed a new interlayer technol. that attain 50% redn. in capacitance and keep good process compatibility with current Chem. Mech. Polishing (CMP) based multi-level metalization (MLM) process. This technol. uses fluorinated amorphous C (a-C:F) with a ***dielec*** . const. of 2.3, sandwiched between layers of SiO2, which are formed in sequential by high d. ***plasma*** -CVD (HDP-CVD) technique. Top SiO2 layer assures O ***plasma*** resistance during via ***etching*** , metal ***etching*** , and ***resist*** removal.
CC ***76-3*** (Electric Phenomena)
IT ***Dielectric*** films
MOS devices
Semiconductor device fabrication
(fluorinated amorphous carbon interlayer technol. for quarter micron devices)
IT ***Plasma*** ***etching***
Selective ***etching***
(in fluorinated amorphous carbon interlayer technol. for quarter

micron devices)
IT ***Dielectric*** constant
(of fluorinated amorphous carbon interlayer)
IT Amorphous films
Plasma chemical vapor deposition
(***plasma*** CVD of fluorinated amorphous carbon interlayer between silica layers)
IT ***Etching*** ***masks***
(***silica*** ; in fluorinated amorphous carbon interlayer technol. for quarter micron devices)
IT 7631-86-9, Silica, processes 7631-86-9D, Silica, silicon-excess
(***plasma*** CVD of fluorinated amorphous carbon interlayer between silica layers)
IT 75-73-0, Carbon tetrafluoride ***7782-44-7*** , Oxygen, uses
(***plasma*** ***etchant*** ; in fluorinated amorphous carbon interlayer technol. for quarter micron devices)

L42 ANSWER 11 OF 28 HCA COPYRIGHT 1999 ACS
127:57896 WSi2/polysilicon gate ***etching*** using TiN ***hard*** ***mask*** in conjunction with ***photoresist*** . Tabara, Suguru (Group 1, Semiconductor Division, Process Development Department, YAMAHA Corporation, Shizuoka, 438-01, Japan). Jpn. J. Appl. Phys., Part 1, 36(4B), 2508-2513 (English) 1997. CODEN: JAPNDE. ISSN: 0021-4922. Publisher: Japanese Journal of Applied Physics.
AB We found that the selectivity between TiN and poly-Si film was high enough in Cl2/ ***O2*** ***plasma*** to use TiN as an ***etching*** mask for poly-Si gate ***etching*** . We also discovered that the ***oxidn*** . of the TiN surface is the reason why TiN serves as an ***etching*** mask in poly-Si ***etching*** using Cl2/ ***O2*** ***plasma*** . By using a TiN ***hard*** ***mask*** in conjunction with a thin ***photoresist*** , we were able to reduce electron shading damage. The low aspect ratio of the space of a line-and-space (L&S) ***pattern*** is the major reason for the redn. in electron shading damage in this TiN mask process. A portion of the TiN surface on which no charge up occurs is exposed to the ***plasma*** during the overetch step because ***photoresist*** is eroded by ion bombardment. This is an another reason for the reduced electron shading damage.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): ***76***
ST tungsten silicate polysilicon gate ***plasma*** ***etching*** ; titanium nitride ***etching*** mask polysilicon gate; electron shading damage redn ***plasma*** ***etching*** ; MOS capacitor titanium nitride ***etching*** mask
IT MOS capacitors
Plasma ***etching***
(titanium nitride as ***etching*** mask for poly-Si gate ***etching***)
IT ***Photoresists***
(titanium nitride in conjunction with ***photoresist*** as ***etching*** mask for poly-Si gate ***etching***)
IT 13463-67-7, Titania, processes
(***plasma*** ; titanium nitride as ***etching*** mask for poly-Si gate ***etching***)
IT ***7782-44-7*** , Oxygen, uses 7782-50-5, Chlorine, uses
(***plasma*** ; titanium nitride as ***etching*** mask for poly-Si gate ***etching***)

IT 25583-20-4, Titanium nitride(TiN)
(polycryst.; titanium nitride as ***etching*** mask for poly-Si gate ***etching***)
IT 7440-21-3, Silicon, processes
(polycryst.; titanium nitride as ***etching*** mask for poly-Si gate ***plasma*** ***etching***)
IT 12039-88-2, Tungsten silicide(WSi2)
(titanium nitride as ***etching*** mask for poly-Si gate ***etching***)

L42 ANSWER 12 OF 28 HCA COPYRIGHT 1999 ACS
126:286387 Platinum ***etching*** in an inductively coupled ***plasma*** . Park, S.-G.; Lee, J. G.; Choi, Y. S.; Lee, S. H.; Yoo, W. J.; Jung, C. O.; Koh, Y. B.; Lee, M. Y. (Microelectronics Research Lab, Inha University, Inchon, 402-751, S. Korea). ESSDERC'96, Proc. Eur. Solid State Device Res. Conf., 26th, 631-634. Editor(s): Baccarani, Giorgio; Rudan, M. Editions Frontieres: Gif-sur-Yvette, Fr. (English) 1996. CODEN: 64CSAW.
AB Inductively coupled ***plasma*** as a high d. ***plasma*** source and Cl2 as main process gas are tested for ***etching*** of Pt thin films. Optical emission spectra show the possible compd. formation of Pt with Cl, which is an evidence of ion-assisted chem. reaction. Addn. of oxygen to Cl2 ***plasma*** enhances the selectivity to ***hard*** SiO2 ***mask*** to more than 2.0 while maintaining Pt ***etch*** rate higher than 200 nm/min. ***Patterning*** of half micron Pt lines is demonstrated.
CC ***76-11*** (Electric Phenomena)
Section cross-reference(s): 56
ST platinum ***etching*** inductively coupled ***plasma*** ; chlorine ***plasma*** ***etching*** platinum silica mask
IT ***Plasma*** ***etching***
(platinum ***etching*** in an inductively coupled ***plasma***)
IT ***7782-44-7*** , Oxygen, uses
(chlorine ***plasma*** ; platinum ***etching*** in an inductively coupled ***plasma***)
IT 7440-06-4, Platinum, processes
(***etching*** in an inductively coupled ***plasma***)
IT 7631-86-9, Silica, uses
(mask; platinum ***etching*** in an inductively coupled ***plasma***)
IT 7782-50-5, Chlorine, uses
(***plasma*** ; platinum ***etching*** in an inductively coupled ***plasma***)

L42 ANSWER 13 OF 28 HCA COPYRIGHT 1999 ACS
126:271072 Post-gate LOCOS in manufacture of an integrated circuit. Sun, Yu; Liu, Yowjuang W. (Advanced Micro Devices, Inc., USA). U.S. US 5612249 A 19970318, 21 pp. (English). CODEN: USXXAM. APPLICATION: US 96-645844 19960514.
AB A gate oxide is grown on a Si substrate, and then poly or amorphous Si is deposited. A thin layer of PECVD or LPCVD oxide is deposited on the poly, and LPCVD nitride is then deposited as a ***hard*** ***mask*** . A device active area is defined by ***photoresist*** mask and ***plasma*** ***etch*** . The layers may either be ***etched*** down to the Si surface, or the Si surface may be further ***etched*** to create a recessed Si region. An oxide layer is grown on the exposed sidewalls of the poly, and another layer of nitride is deposited. The nitride is ***etched*** to form a nitride spacer, and a field oxide is grown.

A field isolation implant is formed, followed by stripping the
nitride spacer. The oxide layer is removed, reexposing the poly.
Another layer of poly and a WSi film are deposited, and the gate and
interconnects are defined by applying a gate mask and ***etch***
. Alternatively, self-aligned silicide gate, junction, and
interconnect can be formed without using WSi by depositing Ti after
the gate is defined. N-LDD and P-LDD implants are performed by
masks, followed by an oxide spacer being formed. N+ and P+
junctions are then formed by sep. masks and implants.
IC ICM H01L021-76
NCL 437069000
CC ***76-3*** (Electric Phenomena)
IT Ion implantation
Sputter ***etching***
(in manuf. of integrated circuits)
IT ***Plasma*** chemical vapor deposition
(of oxide layers in manuf. of integrated circuits)
IT ***Oxidation***
(post-gate LOCOS in manuf. of integrated circuits)

L42 ANSWER 14 OF 28 HCA COPYRIGHT 1999 ACS
125:343965 Reactive ion ***etching*** of the fluorinated polyimide
film. Lee, Y. K.; Murarka, S. P. (Cent. Int. Electron. Electronics
Manuf., Rensselaer Polytech. Inst., Troy, NY, 12180, USA). Mater.
Res. Soc. Symp. Proc., 427(Advanced Metallization for Future ULSI),
455-461 (English) 1996. CODEN: MRSPDH. ISSN: 0272-9172.
AB Conditions affecting the ***etch*** rate of fluorinated
polyimide films with RF ***plasma*** using oxygen or
fluorine-contg. ***oxygen*** , including ***gas*** flow rate
and compn., were detd., to establish optimum procedures for
fabrication of integrated circuits and packaging of electronic
devices. The ***etch*** rate increased linearly with the RF
power and ***oxygen*** ***gas*** flow. Satn. at high oxygen
flow rate, is indicative of steady state reaction at the
polyimide-oxygen interface. However, the ***etch*** rate
increased when CF4 is added to oxygen, up to about 10% CF4 in
O2 , and then decreased, to level independent of CF4 concn.
The ***etch*** selectivity of PECVD [***plasma*** enhanced
chem. vapor deposition] Si3N4 and PETEOS [***plasma*** -enhanced
tetraethylorthosilicate] ***hard*** ***masks*** against the
fluorinated polyimide was detd. Both, PECVD Si3N4 and PETEOS are
excellent ***hard*** ***masks*** for pattering polyimides.
The trench profile of the polyimide film also was examd. by
patterning and ***etching*** the different trench sizes
in fluorinated polyimide. This fluorinated polyimide can be
etched with oxygen or fluorine contg. oxygen ***plasma***
.
CC ***76-2*** (Electric Phenomena)
Section cross-reference(s): 38
ST fluoropolyimide ***plasma*** ***etching*** oxygen
fluoromethane; silicon nitride mask ***plasma*** ***etching***
fluoropolyimide; tetraethylorthosilicate mask ***etching***
fluoropolyimide ***patterning***
IT Electronic device packaging
Plasma
(reactive ion ***etching*** of fluorinated polyimide film and
selectivity of Si3N4 and PETEOS ***hard*** ***masks***)
IT Sputtering
(***etching*** , ***patterning*** ; reactive ion
etching of fluorinated polyimide film and selectivity of

Si3N4 and PETEOS ***hard*** ***masks***)

IT Polyimides, processes
(fluorine-contg., reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

IT Electric circuits
(integrated, reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

IT Fluoropolymers
(polyimide-, reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

IT ***Etching***
(sputter, ***patterning*** ; reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

IT 78-10-4
(***plasma*** -enhanced; reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

IT 75-73-0, Carbon fluoride (CF4) ***7782-44-7*** , Oxygen, uses
12033-89-5, Silicon nitride, uses
(reactive ion ***etching*** of fluorinated polyimide film and selectivity of Si3N4 and PETEOS ***hard*** ***masks***)

L42 ANSWER 15 OF 28 HCA COPYRIGHT 1999 ACS

125:314087 Trench isolation technology for high performance complementary bipolar devices. Brown, Kevin C.; Bracken, Chris; Bashir, Rashid; Egan, Kulwant; DeSantis, Joe; Kabir, Abul Ehsanul; Yindeepol, Wipawan; McGregor, Joel; Prasad, S. J.; et al. (Analog Process Technology Development, National Semiconductor Corporation, Santa Clara, CA, 95052-8090, USA). Proc. SPIE-Int. Soc. Opt. Eng., 2875(Microelectronic Device and Multilevel Interconnection Technology II), 48-61 (English) 1996. CODEN: PSISDG. ISSN: 0277-786X.

AB A trench isolation architecture for a low voltage (<15V), high frequency, complementary bipolar process technol. was developed. This technol. features shallow and deep trench isolation with a min. design rule of 1.0.mu., along with a zero encroachment deposited field oxide. Trench ***etch*** process results suggest a mechanism whereby, depending on the amt. of exposed Si, the ***plasma*** can either be considered Si deficient or O deficient. Black Si formation during trench ***etching*** was eliminated with an in situ removal of the ***photoresist*** after the ***hard*** ***mask*** oxide was defined. Terrain isolation process simulation results are more accurate in depicting actual wafer processing structures than Tsuprem-4. Initial bipolar device characteristics are reported that illustrate the integration of the introduced PlaTOx device isolation architecture. Realized ft/fmax are 6.3/9.5 GHz for NPN, and 3.8/8.2 GHz for PNP transistors.

CC ***76-14*** (Electric Phenomena)
Section cross-reference(s): 74

ST trench ***etch*** bipolar integrated circuit transistor

IT Electric potential
Etching
Plasma
Transistors
(trench isolation process for high performance complementary bipolar devices)

IT ***Resists***
(photo-, trench isolation process for high performance complementary bipolar devices)
IT 7440-59-7, Helium, uses ***7782-44-7*** , Oxygen, uses 7783-54-2, Nitrogen fluoride (NF3) 10035-10-6, Hydrogen bromide, uses
(trench ***etching*** for high performance complementary bipolar devices using ***plasma*** contg.)

L42 ANSWER 16 OF 28 HCA COPYRIGHT 1999 ACS
125:290959 Method for ***plasma*** ***etching*** an oxide/polycide structure and manufacture of a semiconductor structure including this method. Costaganna, Pascal; Martinet, Francois (International Business Machines Corp., USA; Ibm France). PCT Int. Appl. WO 9627899 A1 19960912, 25 pp. DESIGNATED STATES: W: JP, KR; RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE. (English). CODEN: PIXXD2. APPLICATION: WO 96-EP922 19960305. PRIORITY: EP 95-480015 19950308; EP 95-480093 19950713.
AB A semiconductor structure including a stack comprised of a cap SiO2 layer, a WSi2 layer, and a bottom polysilicon layer formed on a Si substrate coated with a thin oxide layer is ***patterned*** in a 2-step ***plasma*** process with a ***resist*** stripping/cleaning step between them. After a ***resist*** mask is formed on the structure, the cap SiO2 layer is ***etched*** in a 1st chamber of a multichamber magnetically enhanced reactive ion ***etching*** reactor using CHF3, ***O2*** , and Ar. Then, the semiconductor structure is removed from the reactor. The ***resist*** mask is eliminated by ***O2*** ashing and the wafer cleaned using dil. HF (100:1). Next, the structure is introduced into a 2nd chamber of the RIE reactor, and the WSi2 and polysilicon layers are ***etched*** in sequence using the ***patterned*** cap SiO2 layer as a ***hard*** ***mask*** . A mixt. of HCl, Cl2, and N2, preferably with a few ppm of ***O2*** , is adequate for WSi2 ***etching*** and a mixt. of HCl, He, and He- ***O2*** is adequate for polysilicon ***etching*** . The thin oxide layer is attacked to a very small extent during this step. Finally, the semiconductor structure is removed from the reaction chamber and is ready for subsequent processing. The improved method is substantially contamination-free and only requires 2 reaction chambers instead of 4. The improved ***etching*** method finds extensive application in the semiconductor industry and in particular in the formation of the gate conductor stack in 16-Mbit DRAM chips.
IC ICM H01L021-321
CC ***76-11*** (Electric Phenomena)
ST ***plasma*** ***etching*** oxide polycide structure; semiconductor structure oxide polycide ***plasma*** ***etching***
IT Ashing
(of ***resist*** masks after ***plasma*** ***etching*** of oxide/polycide structures)
IT Semiconductor devices
(***plasma*** ***etching*** of oxide/polycide structures in semiconductor device manuf.)
IT Silicides
Oxides, processes
(***plasma*** ***etching*** of oxide/polycide structures in semiconductor device manuf.)
IT Sputtering
(***etching*** , of oxide/polycide structures in semiconductor

device manuf.)
IT   Sputtering
     (***etching*** , reactive, of oxide/polycide structures in semiconductor device manuf.)
IT   Memory devices
     (random-access, ***plasma*** ***etching*** of oxide/polycide structures in manuf. of)
IT   ***Etching***
     (sputter, of oxide/polycide structures in semiconductor device manuf.)
IT   ***Etching***
     (sputter, reactive, of oxide/polycide structures in semiconductor device manuf.)
IT   7664-39-3, Hydrogen fluoride, processes
     (cleaning by; of semiconductor wafers after ***resist*** mask ashing)
IT   75-46-7, Fluoroform 7440-37-1, Argon, processes 7440-59-7, Helium, processes 7647-01-0, Hydrogen chloride, processes 7727-37-9, Nitrogen, processes ***7782-44-7*** , Oxygen, processes 7782-50-5, Chlorine, processes
     (***plasma*** ***etching*** of oxide/polycide structures in gas mixts. contg.)
IT   12039-88-2, Tungsten disilicide
     (***plasma*** ***etching*** of oxide/polycide structures in semiconductor device manuf.)
IT   7440-21-3, Silicon, processes
     (polycryst.; ***plasma*** ***etching*** of oxide/polycide structures in semiconductor device manuf.)

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125:263275 ***Plasma*** ***etching*** an oxide/polycide structure. Costaganna, Pascal; Martinet, Francois (International Business Machines Corp., USA). Eur. Pat. Appl. EP 731501 A1 19960911, 13 pp. DESIGNATED STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP 95-480015 19950308.
AB   A semiconductor structure including a stack comprised of a cap SiO2 layer, a W silicide layer, and a bottom polysilicon layer formed on a Si substrate coated with a thin oxide layer is ***patterned*** in a 2-step ***plasma*** process with a ***resist*** stripping/cleaning step between them. After a ***resist*** mask is formed on top of the structure, the cap SiO2 layer is ***etched*** as std. in a 1st chamber of a multichamber magnetically enhanced RIE reactor using CHF3, ***O2*** , and Ar. Then the semiconductor structure is removed from the reactor. The ***resist*** mask is eliminated by ***O2*** ashing as std. and the wafer cleaned using dil. HF (100:1). Next, the structure is introduced into a 2nd chamber of the RIE reactor, and the WSi2 and polysilicon layers are ***etched*** in sequence using the ***patterned*** cap SiO2 layer as a ***hard*** ***mask*** with adequate chemistries. A mixt. of HCl, Cl2, and N2 is adequate for W silicide ***etching*** and a mixt. of HCl, He, and He-***O2*** is adequate for polysilicon ***etching*** . The thin oxide layer is attacked to a very small extent during this step. Finally, the semiconductor structure is removed from the reaction chamber and is ready for subsequent processing. The improved ***etching*** method finds extensive application in the semiconductor industry and in particular in the formation of the gate conductor stack in 16-Mbit DRAM chips.
IC   ICM H01L021-321
CC   ***76-3*** (Electric Phenomena)

ST ***plasma*** ***etching*** oxide polycide structure; reactive ion ***etching*** oxide polycide structure; tungsten silicide reactive ion ***etching*** ; silica reactive ion ***etching*** ; polysilicon reactive ion ***etching***

IT Cleaning
(in ***plasma*** ***etching*** of oxide/polycide structures)

IT Ashing
(of ***resist*** masks after reactive ion ***etching*** of oxide/polycide structures)

IT Silicides
Oxides, processes
(***plasma*** ***etching*** oxide/polycide structures)

IT Semiconductor devices
(***plasma*** ***etching*** oxide/polycide structures in)

IT Sputtering
(***etching*** , of oxide/polycide structures)

IT Sputtering
(***etching*** , reactive, magnetically enhanced; of oxide/polycide structures)

IT Memory devices
(random-access, reactive ion ***etching*** of oxide/polycide structures in)

IT ***Etching***
(sputter, of oxide/polycide structures)

IT ***Etching***
(sputter, reactive, magnetically enhanced; of oxide/polycide structures)

IT 7664-39-3, Hydrogen fluoride, processes
(cleaning by; of semiconductor wafers after reactive ion ***etching*** of oxide/polycide structures)

IT 7440-21-3, Silicon, processes
(polycryst.; ***plasma*** ***etching*** oxide/polycide structures)

IT 75-46-7, Fluoroform
(reactive ion ***etching*** of oxide/polycide structures in)

IT 7440-37-1, Argon, processes 7440-59-7, Helium, processes 7647-01-0, Hydrogen chloride, processes 7727-37-9, Nitrogen, processes ***7782-44-7*** , Oxygen, processes 7782-50-5, Chlorine, processes
(reactive ion ***etching*** of oxide/polycide structures in gas mixts. contg.)

123:304580 Manufacture of semiconductor devices involving dry ***etching*** of ruthenium dioxide for capacitor bottom electrode. Kajana, Kyonori (Nippon Electric Co, Japan). Jpn. Kokai Tokkyo Koho JP 07221197 A2 19950818 Heisei, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 94-9012 19940131.

AB The manuf. involves forming a capacitor bottom electrode and an insulating film: depositing a RuO2 film, an O ***plasma*** -resistant film, and a ***photoresist*** film in the order, patterning the ***photoresist*** film, patterning the O ***plasma*** -resistant film with the ***photoresist*** mask, O ***plasma*** -reactive ion ***etching*** of the RuO2 film with the O ***plasma*** -resistant mask to form a bottom electrode, removing the O ***plasma*** -resistant mask by dry ***etching*** , and depositing an insulating film of high ***dielecs*** . The O ***plasma*** -resistant film may comprise SOG (spin-on-glass), TiN, polysilicon, amorphous Si, ***plasma***

SiN, Al, or Cr. The capacitor insulating film may comprise SrTiO3 or BaxSr1-xTiO3.
IC ICM H01L021-8242
ICS H01L027-108; H01L027-04; H01L021-822
CC ***76-3*** (Electric Phenomena)
ST semiconductor capacitor ruthenium dioxide ***etching*** ; dry ***etching*** ruthenium dioxide capacitor; oxygen ***plasma*** RIE ruthenium dioxide
IT Semiconductor devices
(manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT Sputtering
(***etching*** , ion-beam, reactive, manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT ***Etching***
(sputter, ion-beam, reactive, manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT 12060-59-2, Strontium titanate 37305-87-6, Barium strontium titanate
(capacitor insulating film; manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT 7429-90-5, Aluminum, uses 7440-21-3, Silicon, uses 7440-47-3, Chromium, uses 7631-86-9, ***Silica*** , uses 12033-89-5, Silicon nitride (Si3N4), uses 12039-70-2, Titanium silicide (TiSi) 25583-20-4, Titanium ***nitride*** (TiN)
(***etching*** ***mask*** ; manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT 12036-10-1, Ruthenium dioxide
(manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)
IT ***7782-44-7*** , Oxygen, uses
(manuf. of semiconductor devices involving oxygen ***plasma*** RIE of ruthenium dioxide for capacitor bottom electrode)

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122:175483 Quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist*** . Engelhardt, M.; Scheler, U. (Siemens AG, Munich, D-81730, Germany). Proc. - Electrochem. Soc., 94-20(Proceedings of the Tenth Symposium on Plasma Processing, 1994), 213-23 (English) 1994. CODEN: PESODO. ISSN: 0161-6374.
AB Quarter-micron polysilicon lines and space ***patterns*** and isolated lines were fabricated with MERIE using an SiO2 ***hard*** ***mask*** with and without a top layer of chem. amplified i-line bilayer ***resist*** . The ***plasma*** process used to structurize the SiO2 film was found to contribute appreciably to the CD gain obsd. after the combined oxide and polysilicon ***etching*** . The CD gain obtained with both types of masks could be successfully reduced by decreasing the thickness of the ***hard*** ***mask*** layer and by an optimization of the ***plasma*** ***etch*** process used to structurize the ***hard*** ***mask*** layer. During overetch oxide deposition on gate oxide or gate oxide erosion was taking place for the same set of process parameters dependent on whether an oxide layer or a ***resist*** -on-oxide sandwich was used as ***etching*** mask resp. Both the oxide deposition and gate oxide erosion were minimized by process parameter optimizations. A substrate damage

evaluation shows that UV radiation damage during polysilicon overetches with MERIE is significantly smaller than with a high d. dual frequency tool.
CC ***76-3*** (Electric Phenomena)
ST quarter micron silicon MERIE ***etch*** ***resist***
IT ***Resists***
(quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist***)
IT Sputtering
(***etching*** , reactive, magnetically enhanced; quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist***)
IT ***Etching***
(sputter, reactive, magnetically enhanced; quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist***)
IT 7440-21-3, Polysilicon, processes 7631-86-9, Silica, processes
(quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist***)
IT ***7782-44-7*** , Oxygen, reactions 7782-50-5, Chlorine, reactions 10035-10-6, Hydrogen bromide, reactions
(quarter-micron polysilicon MERIE using CARL i-line bilayer ***resist***)

L42 ANSWER 20 OF 28 HCA COPYRIGHT 1999 ACS
121:269804 Selective ***etching*** of polysilicon to gate oxide. Keller, David J. (Micron Semiconductor, Inc., USA). U.S. US 5346586 A 19940913, 7 pp. (English). CODEN: USXXAM. APPLICATION: US 92-996074 19921223.
AB In semiconductor device manuf., a method of ***etching*** a polysilicon layer to a gate oxide in a semiconductor structure is provided. The method is performed in situ in a ***plasma*** ***etching*** chamber. Initially, an oxide ***hard*** ***mask*** is formed on the semiconductor structure by ***etching*** a deposited oxide layer through a ***photoresist*** mask. The ***photoresist*** mask is then stripped in the same ***etching*** chamber using a high-pressure ***O3*** ***plasma*** . With the ***photoresist*** mask stripped from the semiconductor structure, the polysilicon layer can be ***etched*** through the oxide ***hard*** ***mask*** to the gate oxide with a high ***etch*** selectivity.
IC ICM H01L021-00
NCL 156656000
CC ***76-3*** (Electric Phenomena)
ST ***etching*** polysilicon gate oxide; ***photoresist*** stripping ***ozone*** ***plasma***
IT Semiconductor devices
(selective ***etching*** of polysilicon to gate oxide in semiconductor device manuf.)
IT Sputtering
(***etching*** , selective ***etching*** of polysilicon to gate oxide in semiconductor device manuf.)
IT ***Etching***
(sputter, selective ***etching*** of polysilicon to gate oxide in semiconductor device manuf.)
IT 7631-86-9, Silica, uses
(gate oxide; selective ***plasma*** ***etching*** of polysilicon and silicide layers to)
IT 10028-15-6, ***Ozone*** , reactions
(***plasma*** ; ***photoresist*** stripping by)
IT 7440-21-3, Silicon, uses

(polycryst.; selective ***etching*** of polysilicon to gate oxide in semiconductor device manuf.)

IT 12627-41-7, Tungsten silicide
(selective ***plasma*** ***etching*** of polysilicon and silicide layers to gate oxide in semiconductor device manuf.)

IT 75-46-7, Trifluoromethane 75-73-0, Carbon fluoride (CF4)
2551-62-4, Sulfur fluoride (SF6) 7440-59-7, Helium, reactions
7726-95-6, Bromine, reactions 7782-41-4, Fluorine, reactions
7782-50-5, Chlorine, reactions 10035-10-6, Hydrogen bromide, reactions
(selective ***plasma*** ***etching*** of polysilicon and silicide layers to gate oxide in semiconductor device manuf.)

L42 ANSWER 21 OF 28 HCA COPYRIGHT 1999 ACS

113:183104 Formation of interlayer insulating films. Masuda, Yoji; Yamamoto, Hiroshi; Sawada, Kazuyuki (Matsushita Electric Industrial Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 02166737 A2 19900627 Heisei, 8 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 88-322678 19881221.

AB The title process comprises steps of (1) formation of a SiO2 and an optional Si3N4 film on the substrate on which wiring is made; (2) formation of a patterned ***resist*** film on the insulating film by removing the ***resist*** film partly or entirely optionally leaving <0.5 .mu.m in thickness on the insulating film between the wiring; (3) optional ***etching*** of the Si3N4 film using the ***resist*** film as a mask; (4) ***etching*** of the SiO2 film at a rate at 0.5-2.times. that of the ***resist*** film and removal of the ***resist*** film, or removal of the ***resist*** film and ***etching*** of the SiO2 film at a rate 0.5-2.times. that of the Si3N4 film and removal of the Si3N4 film; and (5) deposition of a SiO2 film. The overhang of the SiO2 film on the metal wiring is changed to tapered forms. The SiO2 film was deposited by ***plasma*** chem. vapor deposition and ***etched*** by CF4- ***O2*** .

IC ICM H01L021-3205
ICS H01L021-302; H01L021-90

CC ***76-10*** (Electric Phenomena)
Section cross-reference(s): 75

ST interlayer insulating film integrated circuit; ***silica*** film selective ***mask*** ***etching***

IT Electric insulators and ***Dielectrics***
(interlayer films, prepn. of)

IT ***Etching***
(selective, ***mask*** , of ***silica*** films in formation of interlayer insulating films)

IT 7631-86-9, ***Silica*** , reactions
(selective ***mask*** ***etching*** of, in formation of interlayer insulating films)

L42 ANSWER 22 OF 28 HCA COPYRIGHT 1999 ACS

110:32424 Characterization of ***etching*** of silicon dioxide and ***photoresist*** in a fluorocarbon ***plasma*** . Karulkar, Pramod C.; Wirzbicki, Mark A. (Lincoln Lab., Massachusetts Inst. Technol., Lexington, MA, 02173-0027, USA). J. Vac. Sci. Technol., B, 6(5), 1595-9 (English) 1988. CODEN: JVTBD9. ISSN: 0734-211X.

AB Reactive-ion ***etching*** of SiO2 and pos. ***photoresist*** in CHF3-C2F6- ***O2*** -He ***plasma*** in a parallel-plate ***etcher*** was studied using the response surface exptl. design procedure. The exptl. results are reproducible within 5%. Anal. expression for the dependence of the ***etch*** rates on the

plasma parameters (O concn., pressure, rf power) are obtained. Detailed contour maps of the behavior of the ***etch*** rates as functions of the ***plasma*** parameters are prepd. from the analytic expressions. Calcd. ***etch*** rates are within 10% of the measured value at a large no. of points in the range of the parameters explored. Using the results of this study it has been possible to ***etch*** contact holes with a variety of sidewall slopes. Predictability of the ***etch*** rates from the anal. expressions for ***resist*** and SiO2 also provided great flexibility while planarizing a ***dielec*** . over patterned Al and ***etching*** of vias in the planarized but unevenly thick ***dielec*** .

CC ***76-11*** (Electric Phenomena)
Section cross-reference(s): 67

ST reactive ion ***etching*** silica ***photoresist*** ; fluoroform ion ***etching*** silica ***photoresist*** ; fluoropropane ion ***etching*** silica ***photoresist*** ; oxygen ion ***etching*** silica ***photoresist*** ; kinetics ***etching*** silica ***photoresist*** ; via ***etching*** insulator aluminum

IT Electric conductors
(aluminum, reactive ion ***etching*** of silica patterns on)

IT ***Resists***
(for reactive ion ***etching*** of silica)

IT Electric insulators and ***Dielectrics***
(silica, reactive ion ***etching*** of)

IT Sputtering
(***etching*** , ion-beam, reactive, of silica with ***photoresist***)

IT Sputtering
(***etching*** , reactive, of silica with ***photoresist***)

IT Kinetics of ***etching***
(sputter, ion-beam, of silica)

IT ***Etching***
(sputter, ion-beam, reactive, of silica with ***photoresist***)

IT ***Etching***
(sputter, reactive, of silica with ***photoresist***)

IT 7429-90-5, Aluminum, uses and miscellaneous
(elec. conductor, reactive ion ***etching*** of silica patterns on)

IT 7631-86-9, Silica, reactions
(***etching*** of, by reactive ions)

IT ***7782-44-7*** , Oxygen, reactions
(reactive ion ***etching*** of silica with)

IT 75-46-7, Fluoroform 76-16-4, Hexafluoroethane 7440-37-1, Argon, uses and miscellaneous 7440-59-7, Helium, uses and miscellaneous
(reactive ion ***etching*** of silica with)

IT 89591-73-1
(reactive ion ***etching*** of ***silica*** with ***mask*** of)

L42 ANSWER 23 OF 28 HCA COPYRIGHT 1999 ACS

103:170743 Process for forming isolating trenches in integrated circuit devices. Goth, George Richard; Hansen, Thomas Adrian; Villetto, Robert Thomas, Jr. (International Business Machines Corp. , USA). Eur. Pat. Appl. EP 146789 A2 19850703, 30 pp. DESIGNATED STATES: R: DE, FR, GB. (English). CODEN: EPXXDW. APPLICATION: EP 84-114122 19841123. PRIORITY: US 83-566593 19831229.

AB An improved image-transfer technique is described for forming deep isolation trenches, including the steps of: first, applying an org. underlayer, preferably ***photoresist*** , over the trench-defining masking layer, followed by ***plasma*** deposition of a nitride or oxide layer over the org. underlayer; next, applying a conventional imaging layer of ***photoresist*** over the ***plasma*** -deposited layer, and by utilizing conventional photolithog. techniques, creating a pattern of openings in the ***plasma*** -deposited layer; thirdly, performing reactive ion ***etching*** , preferably using CF4, of the ***plasma*** -deposited layer, followed by a highly selective reactive ion ***etching*** of the org. underlayer. This is preferably accomplished by the use of ***O2*** as the ***etchant*** . The desired vertical walls (>85.degree.) are achieved by virtue of the high ***etch*** rate ratio (100 to 1) operative between the org. underlayer (e.g. ***resist***) and, for example, the ***plasma*** nitride; a reactive ion ***etching*** , again by CF4, of the ***masking*** ***SiO2*** layer and the field ***dielec*** . layers operates to transfer the trench-mask image so as to maintain vertical side walls through the ***dielec*** . layers. After stripping of the remaining underlayer by using an ***O2*** ash, the Si trench is reactive ion ***etched*** in an SF6 (2.5%), Cl2 (7.5%), He (90%) mixt. A redn. in device size of .apprx.40% is achievable in monolithic integrated circuit structures. Image resoln. of min. trench widths of .apprx.2.5 .mu.m is possible. The undesirable slope normally obtained in the field ***dielec*** . layers at the top of the trenches is avoided. The photo-limited yield of trench mask levels is improved by avoiding the normally occurring particulate contamination in the relatively thick SiO2 layers by forming the ***masking*** ***SiO2*** layer by ***plasma*** deposition.

IC ICM H01L021-308
ICS H01L021-306; H01L021-76

CC ***76-3*** (Electric Phenomena)

IT ***Etching***
(of isolation trenches for integrated circuits)

IT Electric insulators and ***Dielectrics***
(trenches, in integrated circuits)

IT 2551-62-4 ***7782-44-7*** , uses and miscellaneous 7782-50-5, uses and miscellaneous
(***etchant*** , in trench formation for integrated circuits)

IT 7440-59-7, uses and miscellaneous
(***etching*** atm. contg., in trenching for integrated circuits)

IT 75-73-0
(***etching*** by, for trenches in integrated circuits)

IT 7631-86-9, uses and miscellaneous 12033-89-5, uses and miscellaneous
(***plasma*** deposition and ***etching*** of, in formation of trenches for integrated circuits)

L42 ANSWER 24 OF 28 HCA COPYRIGHT 1999 ACS

102:16156 Inter-component isolation of integrated circuits. (Mitsubishi Electric Corp., Japan). Jpn. Kokai Tokkyo Koho JP 59126649 A2 19840721 Showa, 4 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 83-2072 19830108.

AB Isolation is achieved without bird-beak formation by masking the Si with electron-beam ***resists*** , ***etching*** grooves, depositing the ***SiO2*** film, ***masking*** over the grooves, ***etching*** until side ***etching*** occurs, and

removing the ***resist*** masks.
IC H01L021-76; H01L021-306
CC ***76-10*** (Electric Phenomena)
IT ***Etching***
(of silicon for isolation of integrated-circuit component)
IT Electric insulators and ***Dielectrics***
(coatings, silica, for isolation of integrated-circuit component)
IT Sputtering
(***etching*** , of silicon and silica for isolation of integrated-circuit component)
IT ***Etching***
(ion-beam, reactive, of silicon and silica for isolation of integrated-circuit component)
IT ***Etching***
(sputter, of silicon and silica for isolation of integrated-circuit component)
IT 7664-39-3, uses and miscellaneous
(***etchant*** , for isolation of integrated-circuit components)
IT 75-73-0
(***etchant*** , for isolation of silicon integrated-circuit components)
IT 1333-74-0, uses and miscellaneous ***7782-44-7*** , uses and miscellaneous
(***plasma*** ***etchant*** contg., for isolation of integrated-circuit components)

L42 ANSWER 25 OF 28 HCA COPYRIGHT 1999 ACS
101:47333 Integrated-circuit isolation. (Suwa Seikosha Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 59035446 A2 19840227 Showa, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 82-145947 19820823.
AB Integrated-circuit isolation is achieved with high precision by implanting n-Si with B to form a p-Si region, coating with SiO_2 and ***SiN*** , pos. ***resist*** ***masking*** ***plasma*** ***etch*** patterning only the SiN with CF_4, adding ***O2*** to ***plasma*** , removing the ***resist*** , heating in N, superimposing a neg. 2-layer ***resist*** , patterning the ***resist*** , and implanting B.
IC H01L021-76; H01L021-312; H01L027-08
ICA H01L021-265
CC ***76-3*** (Electric Phenomena)
IT Electric insulators and ***Dielectrics***
(silica and silicon nitride, for isolation of integrated circuits)
IT Sputtering
(***etching*** , of silicon nitride with carbon tetrafluoride ***plasma*** for isolation of integrated circuit)
IT Sputtering
(***etching*** , of silicon nitride, in carbon tetrafluoride, for isolation of integrated circuits)
IT Electric circuits
(integrated, isolation of, with silicon ***nitride*** ***mask***)
IT ***Etching***
(sputter, of silicon nitride with carbon tetrafluoride ***plasma*** for isolation of integrated circuit)
IT ***Etching***
(sputter, of silicon nitride, in carbon tetrafluoride, for isolation of integrated circuits)
IT ***7782-44-7*** , uses and miscellaneous

(***plasma*** ***etchant*** from, for silica isolation in integrated circuits)
IT 75-73-0
(***plasma*** ***etchant*** from, for silicon isolation in integrated circuits)

L42 ANSWER 26 OF 28 HCA COPYRIGHT 1999 ACS
101:31945 Silica insulation semiconductor device. (Nippon Electric Co., Ltd., Japan). Jpn. Kokai Tokkyo Koho JP 59028356 A2 19840215 Showa, 3 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 82-138313 19820809.
AB SiO2 insulation which is confined to a precisely defined region is obtained by forming a p+-Si layer epitaxially on p-Si, thermally ***oxidizing*** , ***resist*** masking, ***plasma*** ***etching*** , removing the mask, depositing Si, and removing excess poly-Si from the SiO2 surface.
IC H01L021-76
CC ***76-3*** (Electric Phenomena)
IT ***Etching***
(of silica with hydrofluoric acid in semiconductor-device fabrication)
IT Electric insulators and ***Dielectrics***
(silica, for semiconductor devices with isolated element regions)
IT Sputtering
(***etching*** , of silicon and silica in semiconductor-device fabrication)
IT ***Etching***
(sputter, of silicon and silica in semiconductor-device fabrication)
IT 7664-39-3, uses and miscellaneous
(***etchant*** , for silica in semiconductor devices)
IT 12033-89-5, uses and miscellaneous
(***masks*** , for ***silica*** insulation of semiconductor devices)

L42 ANSWER 27 OF 28 HCA COPYRIGHT 1999 ACS
93:248282 Fabrication of chromium photomasks. (Mitsubishi Electric Corp., Japan). Jpn. Kokai Tokkyo Koho JP 55073047 19800602 Showa, 5 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 78-147491 19781125.
AB A glass support is coated with a ***hard*** ***photomask*** forming layer, then coated with a radiation ***resist*** layer, then the ***resist*** layer is irradiated ***patternwise*** with an electron beam, then the ***hard*** ***photomask*** layer is ion planted with O ions at an energy such that the O ions are implanted only in the area where the ***resist*** layer thickness is reduced by the electron-beam irradn., subsequently the ***resist*** layer is removed, and the photomask forming layer is ***plasma*** ***etched*** in a halogen- ***O*** mixt. ***gas*** to give a photomask. The method is esp. useful for prepg. Cr photomasks.
IC G03C007-00; G03C001-72; G03F001-00; H01L021-308
CC 74-8 (Radiation Chemistry, Photochemistry, and Photographic Processes)
Section cross-reference(s): ***76***
ST photomask fabrication ***plasma*** ***etching*** ; chromium photomask fabrication
IT Photomasks
(chromium, fabrication of, by ***plasma*** ***etching*** after selective O ion implantation)

IT ***Resists***
(electron-beam, for chromium photomask fabrication)
IT 7440-47-3, uses and miscellaneous
(photomasks of, fabrication of, by ***plasma*** ***etching*** after selective O ion implantation)

L42 ANSWER 28 OF 28 HCA COPYRIGHT 1999 ACS
93:214350 Selective ***plasma*** ***etching*** of ***dielectric*** masks in the presence of native oxides of group III-V compound semiconductors. Mogab, Cyril Joseph; Schwartz, Bertram; Hartman, Robert Louis; Koszi, Louis Alex (Western Electric Co., Inc., USA). PCT Int. Appl. WO 8001623 19800807, 16 pp. (English). CODEN: PIXXD2. PRIORITY: US 79-7422 19790129.
AB A selective ***plasma*** ***etching*** process is proposed which removes ***dielec*** . masks from the surfaces of Group IIIA pnictides and their oxides without significant ***etching*** of the pnictide or pnictide oxide. The ***plasma*** contains halocarbons for SiO_2 or Si_3N_4 ***etching*** , and for ***photoresists*** contains halocarbons and O. Thus, a SiO_2 layer on $Al_{0.36}Ga_{0.64}As$ was ***etched*** away with a CF_4 ***plasma*** contg. 8% ***O_2*** at 0.4 torr.
IC H01L021-306
CC ***76-13*** (Electric Phenomena)
ST ***dielec*** mask ***plasma*** ***etching*** ; IIIA pnictide ***etching*** ***dielec*** mask; halocarbon ***plasma*** ***etching*** ***dielec*** mask; oxygen ***plasma*** ***etching*** ***photoresist*** ; carbon fluoride ***etching*** ***silica*** ***mask*** ; aluminum gallium arsenide mask ***etching***
IT Electroluminescent devices
Lasers
(aluminum gallium arsenide semiconductors for, ***plasma*** ***etching*** method for)
IT Group IIIA element pnictides
(***plasma*** ***etching*** of ***dielec*** . masks from)
IT Oxides, reactions
(***plasma*** ***etching*** of ***dielec*** . masks from Group IIIA pnictide)
IT Electric insulators and ***Dielectrics***
Photomasks
Resists
(***plasma*** ***etching*** of, from Group IIIA pnictide and pnictide oxides)
IT Semiconductor devices
(pnictides, ***plasma*** ***etching*** of ***dielec*** . masks for)
IT Hydrocarbons, reactions
(halo, ***plasma*** ***etching*** of, from pnictide semiconductor devices)
IT ***Etching***
(sputter, of ***dielec*** . masks from pnictides and pnictide oxides)
IT 75-73-0 ***7782-44-7*** , properties
(***plasma*** ***etching*** by, of oxide layers on pnictides)
IT 75-46-7 76-16-4
(***plasma*** ***etching*** of ***dielec*** . masks on pnictides by mixt. contg.)
IT 1303-00-0, properties

(***plasma*** ***etching*** of oxide layers from, carbon
tetrafluoride-oxygen mixt. for)

IT 12064-03-8 22398-80-7, properties
(***plasma*** ***etching*** of oxide layers from, carbon
tetrafluoride-oxygen mixt. for)

IT 22831-42-1D, solid solns. with gallium arsenide
(***plasma*** ***etching*** of silica and silicon nitride
from, by carbon tetrafluoride contg. oxygen)

IT 1303-00-0D, solid solns. with aluminum arsenide
(***plasma*** ***etching*** of silica and silicon nitride
from, by carbon tetrafluoride contg. oxygen)

IT 7631-86-9, properties 12033-89-5, properties
(***plasma*** ***etching*** of, from aluminum gallium
arsenide)

=> d l43 1-6 cbib ab hitind

L43 ANSWER 1 OF 6 HCA COPYRIGHT 1999 ACS

130:146095 Feasibility of a CVD ***resist*** based lithography process at 193 nm wavelength. Lee, Carol Y.; Das, Siddartha; Yang, John; Weidman, Tim; Sugiarto, Dian; Nault, Mike; Mui, David; Osborne, Zoe (Intel Corporation, Santa Clara, CA, USA). Proc. SPIE-Int. Soc. Opt. Eng., 3333(Pt. 1, Advances in Resist Technology and Processing XV), 625-633 (English) 1998. CODEN: PSISDG. ISSN: 0277-786X. Publisher: SPIE-The International Society for Optical Engineering.

AB Thin layer imaging can extend the optical lithog. limit down to sub-0.18 .mu.m crit. dimension (CD) with 193 nm wavelength tools. Thin layer imaging can be implemented in a bi-layer approach, in which a ***patterned*** thin layer is transferred into an underlying org. planarizing layer. It can also be implemented in a single-layer ***hardmask*** process, in which a photodefineable oxide precursor is used to directly ***pattern*** a device layer. In the first portion of the authors study, a ***plasma*** polymd. methylsilane (PPMS) bilayer baseline process has been characterized for photospeed, resoln., and line edge roughness (LER). 1500.ANG. Thick organosilane films were ***patterned*** by a photooxidn. process using a 193 nm stepper (NA = 0.6). The process exhibits photospeeds that are easily tuned from 40 to 100 mJ/cm2 in a well-controlled manner by adjusting the PPMS CVD deposition parameters. The process has demonstrated a resoln. of 0.13 .mu.m. We show that the total dry-develop process time is crit. in detg. the lithog. process lattitude, photospeed, resoln. and LER characteristics. The CVD ***resist*** process is most attractive if the thin layer can be directly converted into a thin oxide ***hard*** ***mask*** , useful for transferring the ***pattern*** directly into an underlying device layer. We demonstrate a CVD ***photoresist*** process in which ***patterned*** PPMS is converted into a silicon dioxide ***hardmask*** , and then transferred into underlying amorphous-Si layers with high selectivity. Using this technique, we have successfully demonstrated 0.15 .mu.m resoln. amorphous-Si lines.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

ST photolithog ***plasma*** polymd methylsilane ***photoresist*** chem vapor deposition

IT ***Photoresists***
Plasma chemical vapor deposition
(feasibility of chem. vapor deposited ***photoresist*** based lithog. process at 193 nm wavelength)

IT Photooxidation
Refractive index
Surface roughness
(photospeed and resoln. and line edge roughness of ***plasma*** polymd. methylsilane ***photoresist*** bilayer process)
IT 7631-86-9, Silicon dioxide, processes
(photospeed and resoln. and line edge roughness of ***plasma*** polymd. methylsilane ***photoresist*** bilayer process)
IT 992-94-9, Methylsilane
(photospeed and resoln. and line edge roughness of ***plasma*** polymd. methylsilane ***photoresist*** bilayer process)
IT 105064-43-5, Poly(Methylsilane) 110477-49-1, Poly(Methylsilane)
(photospeed and resoln. and line edge roughness of ***plasma*** polymd. methylsilane ***photoresist*** bilayer process)
IT ***7782-44-7*** , Oxygen, processes 7782-50-5, Chlorine, processes
(***plasma*** ***etch*** ; photospeed and resoln. and line edge roughness of ***plasma*** polymd. methylsilane ***photoresist*** bilayer process)

L43 ANSWER 2 OF 6 HCA COPYRIGHT 1999 ACS
130:73749 ***Etching*** characteristics of a chromium nitride ***hardmask*** for x-ray mask fabrication. Tsuboi, Shinji; Seki, Miyoshi; Suzuki, Katsumi (LSI Basic Research Laboratory, Silicon Systems Research Laboratories, NEC Corporation, Tsukuba, 305-8501, Japan). Proc. SPIE-Int. Soc. Opt. Eng., 3412(Photomask and X-Ray Mask Technology V), 106-111 (English) 1998. CODEN: PSISDG. ISSN: 0277-786X. Publisher: SPIE-The International Society for Optical Engineering.
AB To achieve high-precision x-ray masks, we have developed an extremely low-stress CrN film for use as a ***hardmask*** for x-ray absorber ***etching*** . We have fabricated 0.10-.mu.m line-and-space ***patterns*** in a 0.4-.mu.m-thick Ta-Ge alloy x-ray absorber using a 75-nm-thick CrN ***hardmask*** . The CrN film was ***etched*** by reactive-ion ***etching*** using Cl2 mixed with ***O2*** . The ***etching*** selectivity between the Ta-Ge alloy and the CrN was 13 when using electron-cyclotron-resonance ***plasma*** ***etching*** with SF6 gas. We have also investigated the durability of the CrN film to various acids (e.g., APM(NH3:H2O2:H2O), HPM(HCl:H2O2:H2O), and SPM(H2SO4:H2O2)) which are widely used for Si wafer cleaning processes. The CrN ***etching*** rate for those acids was 3 nm/min or less. These results demonstrate that a sputtered CrN film is an excellent ***hardmask*** for precise x-ray mask fabrication.
CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
ST chromium nitride sputtering x ray mask; ***plasma*** ***etching*** behavior chromium nitride ***hardmask***
IT ***Plasma*** ***etching***
(ECR ***plasma*** ***etching*** selectivity in SF6 of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication against Ta-Ge alloy)
IT ***Etching***
(durability in various acids of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT Sputter deposition
X-ray masks
(***etching*** characteristics of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)

IT Reactive ion ***etching***
(kinetics; ***etching*** characteristics of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT ***Etching*** kinetics
(reactive ion; ***etching*** characteristics of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT Reactive ion ***etching***
(reactive-ion ***etching*** selectivity in Cl2/ ***O2*** of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT 2551-62-4, Sulfur hexafluoride
(ECR ***plasma*** ***etching*** selectivity in SF6 of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication against Ta-Ge alloy)
IT 7647-01-0, Hydrogen chloride, uses
(durability in HCl:H2O2:H2O of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT 7664-93-9, Sulfuric acid, uses
(durability in H2SO4:H2O2 of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT 7664-41-7, Ammonia, uses 7722-84-1, Hydrogen peroxide, uses
(durability in NH3:H2O2:H2O of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT 12705-37-2, Chromium nitride
(***etching*** characteristics of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT ***7782-44-7*** , Oxygen, uses 7782-50-5, Chlorine, uses
(reactive-ion ***etching*** selectivity in Cl2/ ***O2*** of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication)
IT 57854-33-8
(x-ray absorber; ECR ***plasma*** ***etching*** selectivity in SF6 of sputter-deposited CrN ***hardmask*** for x-ray mask fabrication against Ta-Ge alloy)

L43 ANSWER 3 OF 6 HCA COPYRIGHT 1999 ACS
128:121550 Uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks. Dauksher, W. J.; Resnick, D. J.; Smith, S. M.; Pendharkar, S. V.; Tompkins, H. G.; Cummings, K. D.; Seese, P. A.; Mangat, P. J. S.; Chan, J. A. (Motorola, Phoenix Corporate Research Laboratories, Tempe, AZ, 85284, USA). J. Vac. Sci. Technol., B, 15(6), 2232-2237 (English) 1997. CODEN: JVTBD9. ISSN: 0734-211X. Publisher: American Institute of Physics.
AB A low stress silicon oxynitride deposition process has been developed in which the av. stress level can be tailored by adjusting silane flow in the ***plasma*** enhanced chem. vapor deposition reactor. Stress gradients, as might be caused by nonuniform heating or gas distribution, were not found to exist. By vol., the SiON films were found to be approx. 81% silicon dioxide and 19% silicon nitride. Because the films are easily removed in HF, this compn. is ideally suited for use as a ***hard*** ***mask*** ***patterning*** layer on x-ray masks. A reactive ion ***etch*** process employing CHF3, ***O2*** , and Ar gases has demonstrated selectivity to Shipley SNR 200 ***resist*** of better than 3:1. Smooth ***pattern*** transfer into TaSi and TaSiN absorber layers of test features as small as 0.1 .mu.m has been achieved using SiON as the ***hard*** ***mask*** layer. Image placement distortions on the order of 15 nm (3.sigma.) occur

from ***etching*** the SiON films on 64 Mbit SRAM x-ray test masks.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

IT Photomasks (lithographic masks)
Plasma chemical vapor deposition
(uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks)

IT SRAM devices
(uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks for lithog. fabrication of)

IT 75-46-7, Trifluoromethane 7440-37-1, Argon, uses 7664-39-3, Hydrofluoric acid, uses ***7782-44-7*** , Oxygen, uses 12504-61-9, Tantalum silicide(TaSi) 130501-93-8, Megaposit SNR 200 176660-45-0, Tantalum nitride silicide(TaNSi)
(uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks)

IT 7803-62-5, Silane, processes
(uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks)

IT 7631-86-9, Silicon dioxide, uses 11105-01-4, Silicon oxynitride 12033-89-5, Silicon nitride, uses
(uniform low stress oxynitride films for application as ***hard*** ***masks*** on x-ray masks)

L43 ANSWER 4 OF 6 HCA COPYRIGHT 1999 ACS

120:231667 ***Plasma*** deposited organosilicon hydride network polymers as versatile ***resists*** for entirely dry mid-deep-UV photolithography. Joshi, Ajey M.; Weidman, Timothy W.; Johnson, Andrew D.; Miner, John F.; Ibbotson, Dale E. (Bell Lab., ATT, Murray Hill, NJ, 07974, USA). Proc. SPIE-Int. Soc. Opt. Eng., 1925(Advances in Resist Technology and Processing X), 709-20 (English) 1993. CODEN: PSISDG. ISSN: 0277-786X.

AB ***Plasma*** polymd. organosilicon films were used as neg. tone deep-UV ***resists*** in a new all-dry bilayer process. Quarter micron thick organosilane films were photooxidatively ***patterned*** using a GCA deep-UV stepper (248 nm, NA = 0.35 or 0.48) at exposures between 50-200 mJ-cm-2. ***Patterns*** were dry developed with up to 15:1 selectivity by low energy chlorine ***plasma*** ***etching*** employing conditions similar to those used for the selective ***etching*** of polysilicon over SiO2. ***Pattern*** transfer into underlying org. layers was achieved with greater than 50:1 selectivity in a bilayer processing sequence by switching the ***etching*** ***gas*** to ***oxygen*** . The oxide-like ***etch*** resistance of the exposed ***resist*** to subsequent processing allowed direct, high resoln. (0.25-0.35 .mu.m L/S) ***patterning*** of polysilicon and aluminum using appropriate dry ***etch*** chemistries. This provides an attractive, step-saving alternative to current bi- and trilevel schemes involving deposition and multistep ***patterning*** of ***hard*** ***etch*** ***masks*** such as SiO2. Photooxidative ***patterning*** of ***plasma*** deposited organosilane ***resist*** films and subsequent RIE development comprise a new, versatile, entirely dry photolithog. process that is compatible with com. available deposition, exposure and ***plasma*** processing tools, and is well-suited for integration into cluster tool technol.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

ST ***plasma*** polymd organosilicon ***photoresist*** dry photolithog
IT Polysilanes
(***plasma*** deposited , as neg. tone deep-UV ***resists*** for all dry mid-deep-UV photolithog.)
IT Semiconductor devices
(***plasma*** polymd. organosilicon films as neg. tone deep-UV ***resists*** for all-dry bilayer lithog. fabrication of)
IT ***Resists***
(photo-, neg.-working, ***plasma*** deposited organosilicon hydride network polymers as, for all dry mid-deep-UV photolithog.)
IT 137087-68-4, Shipley 1811 154214-84-3, Shipley 1805
(lithog. all-dry bilayer process using ***plasma*** deposited organosilicon hydride network polymer ***resist*** and planarizing layer of)
IT 110477-49-1, Poly(methylsilane) 141552-01-4
(***plasma*** deposited neg. tone deep-UV ***resists*** in all-dry bilayer lithog. process)
IT 992-94-9, Methylsilane 2814-79-1, Ethylsilane
(***plasma*** polymn. of, for application as neg. tone deep-UV ***resists*** in all-dry bilayer lithog. process)
IT 7782-50-5, Chlorine, uses
(***plasma*** , ***etching*** of ***plasma*** deposited organosilicon hydride network polymer ***resist*** by, in dry mid-deep-UV photolithog.)
IT 75-73-0, Carbon tetrafluoride ***7782-44-7*** , Oxygen, uses 10294-34-5, Boron trichloride
(***plasma*** , in all dry mid-deep-UV photolithog. using ***plasma*** deposited organosilicon hydride network polymer ***resist***)

L43 ANSWER 5 OF 6 HCA COPYRIGHT 1999 ACS
119:213694 Semiconductor lasers and manufacture thereof. Tsunoda, Atsuisa; Hosoda, Masahiro; Suga, Yasuo; Takahashi, Kosei; Tani, Kentaro; Matsui, Kaneki (Sharp Corp., Japan). Jpn. Kokai Tokkyo Koho JP 05007050 A2 19930114 Heisei, 9 pp. (Japanese). CODEN: JKXXAF. APPLICATION: JP 91-156592 19910627.
AB The manufg. process of an n-guided AlGaInP-based double-heterojunction laser comprises the steps of forming a ridge waveguide using a ***dielec*** . (Al2O3 or ***SiO2***) ***mask*** , forming a monocryst. GaAs block layer for burying the ridge laterally by MBE which simultaneously forms a polycryst. GaAs layer on the top of the ridge, spin-coating a ***resist*** which bonds to the monocrystal but not to the polycrystal, removing the latter by ***etching*** , removing the ***resist*** by an ***O3*** -UV or an ***O2*** - ***plasma*** ashing, and removing the mask, thus forming a flat contact surface for the upper electrode. The process forms long-life self-aligned lasers with markedly improved throughputs.
IC ICM H01S003-18
CC 73-10 (Optical, Electron, and Mass Spectroscopy and Other Related Properties)

L43 ANSWER 6 OF 6 HCA COPYRIGHT 1999 ACS
116:204264 Vertical oxide ***etching*** without inducing change in critical dimensions. Nagy, Andrew (Adv. Technol. Cent., Motorola, Mesa, AZ, 85202, USA). Opt. Eng. (Bellingham, Wash.), 31(2), 335-340 (English) 1992. CODEN: OPEGAR. ISSN: 0091-3286.

AB An oxide ***etch*** in an AME 8110 is described that gives vertical oxide profiles without change in crit. dimensions relative to the ***resist*** mask. The technique requires the addn. of a polysilicon ***hard*** ***mask*** , and nonpolymg. ***etch*** conditions operating at very low pressures (5 mTorr). This reduces the ***etch*** rate of oxide to approx. half that seen at higher operating pressures (50 mTorr). Although these modifications increase the complexity and reduce the throughput of the process, these drawbacks must be weighted against the improvements obtained in sidewall angle and reproducibility.

CC 74-5 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)

ST lithog vertical silicon oxide ***plasma*** ***etching***

IT Lithography
(vertical oxide ***etching*** process without inducing change in crit. dimensions for)

IT ***Resists***
(photo-, vertical oxide ***etching*** process for, without inducing change in crit. dimensions)

IT 75-46-7 2551-62-4 7440-59-7, Helium, uses ***7782-44-7*** , Oxygen, uses
(***plasma*** , vertical oxide ***etching*** process using, for control of crit. dimensions)

IT 7440-21-3, Silicon, properties
(polycryst., vertical ***plasma*** ***etching*** process for, without inducing change in crit. dimensions)

IT 78-10-4 124024-87-9, System 9
(vertical oxide ***etching*** with good crit. dimension control in relation to)

IT 7631-86-9, Silica, properties
(vertical ***plasma*** ***etching*** process for, without inducing change in crit. dimensions)

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File 347:JAPIO Oct 1976-1999/Feb.(UPDATED 990603)
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File 351:DERWENT WPI 1963-1999/UD=9922;UP=9922;UM=9922
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?ds

Set     Items   Description
S1    1326046   PATTERN?
S2     360904   OXYGENA? OR OZON? OR O2 OR O3 OR (O OR OXYGEN? ?)(2N)(ATMO-
             S? OR ATM? ? OR GAS?? OR GASIF? OR GASEOUS? OR TREAT? OR APPL-
             Y? OR APPLIED OR APPLICATION? OR INJECT? OR INTRODUC?)
S3     884571   OXIDA? OR OXIDN? ? OR OXIDI?
S4    1229209   PLASMA? ?
S5     452472   ETCH? OR MICROETCH? OR CHASE? ? OR CHASING? ? OR ENCHAS? OR
              ENGRAV? OR EMBOSS? OR IMPRINT? OR ENCAUST? OR IMPRESS? OR IN-
             CISE? ? OR INCISING? ?
S6     249425   MASK? OR PHOTOMASK? OR HARDMASK?
S7       4092   HARDMASK? OR S6(2N)(HARD? OR (SILICON OR SI)(N)(OXIDE? ? OR
              DIOXIDE? ?) OR SIO2 OR SILICA? ? OR SIN OR NITRIDE? ? OR OXY-
             NITRIDE? ?)
S8     170648   RESIST OR RESISTS OR PHOTORESIST?
S9     384401   ANISOTROP?
S10      5644   S5(2N)(STOP? OR HALT?) OR ETCHSTOP? OR MICROETCHSTOP?
S11    492934   DIELEC?
S12      1133   (S2 OR S3) AND S4 AND S5 AND S6 AND S8
S13       173   S12 AND S9
S14        16   S12 AND S10
S15        49   S12 AND S11
S16       750   S12 AND S1
S17        68   S12 AND S7
S18        14   S13 AND S15
S19       113   S13 AND S16
S20        32   S15 AND S16
S21        55   S17 AND (S13 OR S15 OR S16)
S22         5   S17 AND S20
S23         5   S21 AND S20
S24        15   S17 AND S13
S25         5   S17 AND S15
S26        53   S17 AND S16
S27         5   S22 OR S23 OR S25
S28        42   (S14 OR S18 OR S24) NOT S27
S29        19   S20 NOT (S27 OR S28)
S30         4   RD S27 (unique items)
S31        39   RD S28 (unique items)
S32        19   RD S29 (unique items)
?t s30/7,de/all; t s31/7,de/all; t s32/ti/all

 30/7,DE/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
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6143325   INSPEC Abstract Number: B1999-03-2550G-037
  Title:  Application  of  plasma  polymerized  methylsilane  for 0.18 mu m
photolithography
  Author(s):  Monget, C.; Lee, C.; Joubert, O.; Amblard, G.; Weidman, T.W.;
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Sugiarto, D.; Yang, J.; Cormont, F.; Inglebert, R.L.
Author Affiliation: France Telecom, CNET, Meylan, France
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3333, pt.1-2 p.366-75
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1998 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1998)3333:1/2L.366:APPM;1-C
Material Identity Number: C574-1998-217
U.S. Copyright Clearance Center Code: 0277-786X/98/$10.00
Conference Title: Advances in Resist Technology and Processing XV
Conference Sponsor: SPIE
Conference Date: 23-25 Feb. 1998 Conference Location: Santa Clara, CA, USA
Language: English Document Type: Conference Paper (PA); Journal Paper (JP)
Treatment: Experimental (X)
Abstract: Plasma polymerized methylsilane resist films (PPMS) have high sensitivity to short wavelength radiation. The photoinduced oxidation of PPMS films exposed in air forms siloxane network material (called PPMSO), allowing dry development by selective etching of the unexposed regions upon treatment with chlorine based plasmas. Negative-tone patterns of oxidized methylsilane thus formed can be consolidated in a standard resist stripper to form SiO/sub 2/ like hard mask patterns. In this work, PPMS films are deposited using a commercial single wafer cluster tool dedicated to dielectric deposition. After exposure at 248 or 193 nm, PPMS development is performed in a commercial high density plasma source etcher. Oxide patterns obtained from PPMS films are used for organic resist patterning (bi-layer application) and gate stack patterning (single layer application). (7 Refs)
Descriptors: cluster tools; oxidation; photoresists; plasma CVD coatings; polymer films; polymerisation; sputter etching; ultraviolet lithography
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30/7,DE/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04215341
E.I. No: EIP95062749519
Title: Applications of plasma-polymerized methylsilane as a resist and silicon dioxide precursor for 193- and 248-nm lithography
Author: Weidman, Timothy W.; Joubert, Olivier P.; Joshi, Ajey M.; Kostelak, Robert L.
Corporate Source: AT&T Bell Labs., Murray Hill, NJ, USA
Conference Title: Advances in Resist Technology and Processing XII
Conference Location: Santa Clara, CA, USA Conference Date: 19950220-19950222
Sponsor: SPIE - Int Soc for Opt Engineering, Bellingham, WA USA
E.I. Conference No.: 22266
Source: Proceedings of SPIE - The International Society for Optical Engineering v 2438 1995. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 496-503
Publication Year: 1995
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-1786-6
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental); A ; (Applications)

Journal Announcement: 9509W4
Abstract: Silicon dioxide is the primary dielectric fabric of silicon integrated circuits, and the need to pattern it accounts for a large percentage of all photolithographic operations. As shrinking device dimensions place extreme demands on both lithography and etching, patterned oxide films are finding yet additional applications as intermediate ?hard masks.' For example, polysilicon gate and metal layers may be etched with greater selectivity and linewidth control through a thin patterned oxide mask, rather than through a thicker photoresist layer (which is used to pattern the oxide and removed before pattern transfer). However, any advantages of such schemes must be weighed against the costs of increasing process complexity. We recently reported a new all-dry photolithographic process based on the plasma deposition and patterning of organosilicon resists. These materials, as best exemplified by plasma polymerized methylsilane (PPMS), possess amorphous Si-Si bond backbone structures and undergo efficient photo-oxidation to give glasslike siloxane network material. Patterns are developed using chlorine plasma etching to selectively remove unexposed regions, providing a negative tone image. In previous papers we have demonstrated the use of these materials in bilevel processes, using oxygen reactive ion etching to transfer patterns in thin PPMS layers through underlying organic planarizing layers. Using 248 nm deep UV exposure tools, such schemes afford sub-0.25 mu m design rule capabilities and are well suited for difficult device topography. Here we describe the discovery and development of a fundamentally different application unique to PPMS: a new direct approach to patterned silicon dioxide. 7 Refs.
Descriptors: *Photolithography; Silanes; Photoresists; Silica; Integrated circuit manufacture; Organometallics; Photochemical reactions; Oxidation; Plasma etching; Reactive ion etching

30/7,DE/3 (Item 1 from file: 351)
DIALOG(R)File 351:DERWENT WPI

010761531
WPI Acc No: 96-258486/199626
Fabricating method for high-density DRAM - with increased capacitance
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: TZENG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
TW 273049	A	19960321	TW 95108966	A	19950828	H01L-027/108	199626 B

Priority Applications (No Type Date): TW 95108966 A 19950828

Abstract (Basic): TW 273049 A
A fabricating method for high-density DRAM with high capacitance comprises: selectively forming field oxide and active area on silicon semiconductor substrate; forming field effect transistor including gate oxide, gate electrode, N- lightly doped region, spacer and source/drain; forming the first isolation, the second isolation and the third isolation; with lithography and plasma etch anisotropically etching the above the first isolation, the second isolation and the third isolation to form node contact of field effect transistor; forming the first polysilicon layer, the fourth isolation and photoresist, in which the first polysilicon layer will fill up the above node contact; with lithography and plasma etch anisotropically etching the above first polysilicon layer and the fourth isolation;

laterally etching the above photoresist to etch partial portion of the above photoresist to expose the fourth isolation locally; with plasma etch anisotropically etching locally exposed the above fourth isolation; removing the above photoresist; with the above fourth isolation as oxidation mask, thermally oxidizing the above first polysilicon layer, that is not covered by the fourth isolation, to form polysilicon thermal SiO2 locally; with phosphorous acid selectively removing the above fourth isolation; with the above polysilicon thermal SiO2 as etch mask and plasma etch anisotropically etching the above first polysilicon layer to one proper depth to from barrel-shaped the first polysilicon layer; with diluted HF removing the above third isolation and polysilicon thermal SiO2 to form storage node of capacitor; forming one second polysilicon layer; with lithography and plasma etch etching the above capacitor dielectric and the second polysilicon layer to pattern top plate of capacitor.

Title Terms: FABRICATE; METHOD; HIGH; DENSITY; DRAM; INCREASE; CAPACITANCE
Derwent Class: U13
International Patent Class (Main): H01L-027/108

30/7,DE/4 (Item 2 from file: 351)
DIALOG(R)File 351:DERWENT WPI

009651320
WPI Acc No: 93-344870/199343
Patterning of conductive metal oxide film on a substrate - by means of an oxygen@ plasma etching process for high resolution features in semiconductor device fabrication
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: MANIAR P; MOGAB J C; MOGAB C J
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5254217	A	19931019	US 92919328	A	19920727	C23F-001/00	199343 B
EP 587990	A2	19940323	EP 93107990	A	19930517	H01L-021/321	199412
JP 6097121	A	19940408	JP 93203645	A	19930726	H01L-021/302	199419
EP 587990	A3	19940524	EP 93107990	A	19930517	C23F-001/00	199525

Priority Applications (No Type Date): US 92919328 A 19920727
Cited Patents: 5.Jnl.Ref; DD 289438; EP 409018; JP 2074006; JP 2177509; JP 58091170; JP 63220524
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5254217	A		7			
EP 587990	A2	E	8			
Designated States (Regional): DE FR GB IT						
JP 6097121	A		7			

Abstract (Basic): US 5254217 A

Fabricating a semiconductor device comprises: providing a substrate having a conductive metal oxide film disposed on it; and etching the oxide film using an oxygen gas plasma.

The conductive metal oxide film comprises an oxide of a metal selected from Ru, Os, Ir and Rh; the ruthenium oxide has a stoichiometric compsn. of 2.03 atoms of O to every one atom of Ru; the etching step is carried out in an RIE apparatus using RF power of 50-400 watts, at a pressure of 1 to 100 militorr; the masking pattern is a hard mask comprising an inorganic material selected from a refractory metal, a refractory metal silicide, a refractory metal oxide

and, polysilicon, or, an organic photoresist material selected from organic photoresist and silylated organic photoresist; a dielectric layer may be formed on the substrate before deposition of the conductive metal oxide film; the RuO2 film is sputter deposited from an Ru target in an O2 ambient.

USE/ADVANTAGE - In the fabrication of a semiconductor device, a method for plasma etching a conductive metal oxide layer to provide a high resolution metal oxide pattern. Particularly, RuO2 features during fabrication of ferroelectric capacitors and other electronic components.

Dwg.0/3

Title Terms: PATTERN; CONDUCTING; METAL; OXIDE; FILM; SUBSTRATE; OXYGEN; PLASMA; ETCH; PROCESS; HIGH; RESOLUTION; FEATURE; SEMICONDUCTOR; DEVICE; FABRICATE

Derwent Class: L03; U11; U12

International Patent Class (Main): C23F-001/00; H01L-021/302; H01L-021/321

International Patent Class (Additional): H01L-021/3205

31/7,DE/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

04099247 INSPEC Abstract Number: A9207-8160C-014, B9204-2550E-026

Title: Effects of O/sub 2/ feed gas impurity on Cl/sub 2/ based plasma etching of polysilicon

Author(s): Zau, G.C.H.; Sawin, H.H.

Author Affiliation: Dept. of Chem. Eng., MIT, Cambridge, MA, USA

Journal: Journal of the Electrochemical Society vol.139, no.1 p. 250-6

Publication Date: Jan. 1992 Country of Publication: USA

CODEN: JESOAN ISSN: 0013-4651

Language: English Document Type: Journal Paper (JP)

Treatment: Experimental (X)

Abstract: The effect of low level, between 0.001 and 10%, O/sub 2/ addition on Cl/sub 2/ based plasma etching of polysilicon in a parallel-plate etcher was investigated. Three strong effects on the etching rate of unmasked polysilicon were observed. Low level O/sub 2/ addition, 0.1-2%, enhanced the etching rate up to four times that of the pristine system. High level O/sub 2/ addition, >or=6%, stopped the etching altogether. Pure Cl/sub 2/ plasma etching rates were enhanced by previous runs with O/sub 2/ addition; a hysteresis effect. The hysteresis was reduced by subsequent system plasma exposure. Running a CF/sub 4/ plasma after O/sub 2/ addition runs cleaned the system and returned it to its pristine state. The stopping of etching at high O/sub 2/ levels was attributed to plasma oxidation of the polysilicon surface; since Cl/sub 2/ plasmas are very selective with respect to oxide, the etching is stopped by the surface oxide. Both the low level O/sub 2/ etching rate enhancement and the hysteresis effect can be attributed to the deposition of an oxychloride film on the etcher surfaces. The oxychloride film, formed by reaction between the etching products and the added O/sub 2/, passivates the interior etcher surfaces against Cl surface recombination, and, therefore, reduces the major Cl loss mechanism. The gas-phase Cl concentration increases, which in turn increases the polysilicon etching rate. These results demonstrate the importance of etcher surface condition and of the etching product deposition. Photoresist masked polysilicon films etched in the same configuration showed similar O/sub 2/ addition dependencies as unmasked polysilicon films. The main difference is that the O/sub 2/ addition effect thresholds are higher with the photoresist mask due to the consumption of the added O/sub 2/ by photoresist etching. Unmasked polysilicon film etched in a commercial etcher. Applied Materials Precision

5000, under magnetically enhanced reactive ion etching configuration, exhibited the same trends as in the parallel-plate research etcher. This indicates that results obtained from the parallel-plate research etcher can be generalized to other configurations. (26 Refs)
Descriptors: elemental semiconductors; oxidation; silicon; sputter etching

31/7,DE/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04909540
E.I. No: EIP98014009925
Title: High rate ECR plasma etching of Cu at room temperature in Cl//2/Ar
Author: Jung, K.-B.; Lee, J.W.; Park, Y.D.; Childress, J.R.; Pearton, S.J.; Ren, F.
Corporate Source: Univ of Florida, Gainesville, FL, USA
Conference Title: Proceedings of the 1996 MRS Fall Symposium
Conference Location: Boston, MA, USA Conference Date: 19961202-19961205
Sponsor: MRS
E.I. Conference No.: 46250
Source: Structure and Evolution of Surfaces Materials Research Society Symposium Proceedings v 440 1997. MRS, Warrendale, PA, USA. p 449-454
Publication Year: 1997
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental)
Journal Announcement: 9803W2
Abstract: The dry etching of Cu generally requires elevated sample temperature in order to promote desorption of the relatively involatile CuCl//x etch products. We have found that the high ion flux present in Electron Cyclotron Resonance plasmas provides efficient sputter-enhanced removal of the copper chloride species at room temperature, and prevents formation of a thick chlorinated selvedge layer. Etch rates up to 4000 angstroms/min are obtained at 1000 W microwave power, 150 W rf power and 1.5 mTorr pressure. The etching is highly anisotropic, and the remaining Cu-related residues may be removed by a post-etch combination of H//2 and O//2 plasma treatments. Photoresist is inadequate as a mask due to reticulation of the resist under the high ion flux, but dielectrics such as SiN//x or SiO//2 are stable. The amount of Cl//2-based residues is found to decrease as the microwave power is increased because of the more efficient sputter desorption at high ion densities. (Author abstract) 16 Refs.
Descriptors: *Plasma etching; Electron cyclotron resonance; Copper compounds; Sputtering; Argon; Anisotropy; Photoresists; Dielectric materials; Silicon nitride; Silica

31/7,DE/3 (Item 1 from file: 62)
DIALOG(R)File 62:SPIN(R)

00670519
Si nanostructures fabricated by electron beam lithography combined with image reversal process using electron cyclotron resonance plasma oxidation
Kurihara, K.; Iwadate, K.; Namatsu, H.; Nagase, M.; Murase, K.
NTT LSI Laboratories, 3-1, Morinosato Wakamiya, Atsugi-shi, Kanagawa 243-01, Japan
J. Vac. Sci. Technol. B; 13(6),2170-2174 (NOV. 1995) CODEN: JVTBD
CPM: 9511-G-0018

Work Type: EXPERIMENTAL

A new image reversal process has been developed for Si nanodevice fabrication that uses electron beam lithography and electron cyclotron resonance (ECR) plasma techniques. This process is based on Si oxidation with an ECR oxygen plasma through the openings in resist mask patterns. Si on SiOSUB(2) is selectively etched by either ClSUB(2)-based ECR plasma etching or KOH anisotropic etching by using a plasma oxide mask. ECR plasma formed silicon oxide with a thickness of 2-3 nm was found to be an excellent etch mask for these etching techniques. Highly directional ECR oxygen plasma keeps the change in the resist linewidth and edge roughness small enough for nanofabrication. Furthermore, the linewidth of reversed Si patterns can be reduced by SFSUB(6) addition to ClSUB(2) in ECR plasma etching. This image reversal process successfully achieves 10-nm-scale Si wires and pillars. (copyright) 1995 American Vacuum Society

Descriptors: ELECTRON BEAMS; ELECTRON CYCLOTRON-RESONANCE; MASKING; SILICON; SILICON OXIDES;

31/7,DE/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05337981
FORMING METHOD FOR PATTERN AND ELEMENT

PUB. NO.: 08-293481 [JP 8293481 A]
PUBLISHED: November 05, 1996 (19961105)
INVENTOR(s): YOSHIMURA TOSHIYUKI
GOTO YASUSHI
OKAZAKI SHINJI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-098251 [JP 9598251]
FILED: April 24, 1995 (19950424)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R004 (PLASMA); R096 (ELECTRONIC MATERIALS -- Glass Conductors); R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS); R100 (ELECTRONIC MATERIALS -- Ion Implantation); R115 (X-RAY APPLICATIONS); R138 (APPLIED ELECTRONICS -- Vertical Magnetic & Photomagnetic Recording)

ABSTRACT

PURPOSE: To suppress the deterioration of a resist mask pattern on the occasion of pattern transfer, even if thin-film resist is used.

CONSTITUTION: A thermally oxidized film 22 is formed as an etching stopper on an Si substrate 21, and a polycrystalline Si 23 being a material to be produced is formed on it. And an oxide film 24 is formed on the surface of the polycrystalline Si 23 by oxidation reaction. After a negative resist 25 is irradiated with an electron beam 26 and developed, the resist pattern is transferred to the oxide film 24. Following this, the polycrystalline Si 23 is etched.

31/7,DE/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05160413
SEMICONDUCTOR DEVICE, AND ITS MANUFACTURE

PUB. NO.: 08-115913 [JP 8115913 A]
PUBLISHED: May 07, 1996 (19960507)
INVENTOR(s): OGAWA TOSHIHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-247979 [JP 94247979]
FILED: October 13, 1994 (19941013)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R004 (PLASMA)

ABSTRACT

PURPOSE: To flatten the multilayer wiring of a semiconductor device small in parasitic capacitance without increasing photolithography masks.

CONSTITUTION: An aluminum film 16, a silicon nitride film 03, and a silicon oxide film 12 are stacked on an insulating film 01, and with photoresists 04A-F as masks, a silicon oxide film 12 and a silicon nitride film 03 are patterned, and silicon oxide films 05B, C, and F are charged and left by application and etch back method only at the section where the interval between silicon oxide films 12 is narrow. Next, an exposed aluminum film 16 is converted into an alumina film by anode oxidation method. Next, after removal of the silicon oxide film 05 and the silicon oxide film 12, with a silicon nitride film 03 as a mask, the aluminum film 16 is patterned by anisotropic dry etching. Next, it is charged with an insulator to flatten itself.

31/7,DE/6 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05090380
PHOTO-EXCITED ETCHING METHOD AND SEMICONDUCTOR DEVICE MANUFACTURED USING THIS METHOD

PUB. NO.: 08-045880 [JP 8045880 A]
PUBLISHED: February 16, 1996 (19960216)
INVENTOR(s): MOCHIJI KOZO
TAKATANI SHINICHIRO
YAMAMOTO SEIJI
TAKAZAWA HIROYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-182161 [JP 94182161]
FILED: August 03, 1994 (19940803)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R002 (LASERS); R004 (PLASMA); R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals)

ABSTRACT

PURPOSE: To realize the micro-processing of semiconductor in high precision without changing pattern shapes and sizes by providing shielding to an etching mask in photo-excited etching.

CONSTITUTION: A channel layer of an InGaAs layer 2, an AlGaAs layer 3, and a GaAs layer 4 is formed on a GaAs substrate 1. On the top of this, a SiO(sub 2) film 5 is formed as a shielding layer. Next, a SiO(sub 2) film 6 is formed, a photoresist film 7 is formed, a pattern of the photoresist film 7 is formed by photo-lithogrpphy, and the SiO(sub 2) film 6 and the

SiN(sub x) film 5 are etched by reactive ion etching with this resist pattern as a mask. Then, the resist film 7 remaining in an oxygen plasma atmosphere 18 eliminated, and the GaAs layer 4 is etched by applying KrF eximer laser. At this time, etching stops automatically on the surface of the AlGaAs layer 3.

31/7,DE/7 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05076301
DRY ETCHING METHOD

PUB. NO.: 08-031801 [JP 8031801 A]
PUBLISHED: February 02, 1996 (19960202)
INVENTOR(s): YANAGIDA TOSHIHARU
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-160965 [JP 94160965]
FILED: July 13, 1994 (19940713)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R003 (ELECTRON BEAM); R004 (PLASMA); R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals)

ABSTRACT

PURPOSE: To selectively perform patterning without using chloro-fluorocarbon gas by etching a compound semiconductor containing no Al and formed on a compound semiconductor layer containing Al with a mixture gas containing an organic compound gas which has a C-O bond and F system.

CONSTITUTION: A compound semiconductor 5 containing no Al and is formed on a compound semiconductor layer 4 containing Al, and over it, a resist mask 6 with a specified opening diameter is formed, and then, dry etched in mixture gas of organic compound gas having C-O bond and F system gas, so that, on the side faces of the resist mask 6 and the semiconductor layer 5, wall protective films 7 are formed. And, when the semiconductor layer 4, substrate, is exposed, a AlF(sub 2) etching stopper layer is formed on the surface. Thus, without raising the particle level and causing any pattern transfer difference, anisotropic processing of the compound semiconductor layer 5 is enabled.

31/7,DE/8 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05043052
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, ITS MANUFACTURE, AND VACUUM PROCESSING USED FOR IT

PUB. NO.: 07-335652 [JP 7335652 A]
PUBLISHED: December 22, 1995 (19951222)
INVENTOR(s): FUKADA MASAO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-130739 [JP 94130739]
FILED: June 14, 1994 (19940614)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R097 (ELECTRONIC MATERIALS -- Metal Oxide

Semiconductors, MOS); R100 (ELECTRONIC MATERIALS -- Ion Implantation)

ABSTRACT

PURPOSE: To provide a technique for easily forming a semiconductor integrated circuit device fitted with a wiring film of high reliability.

CONSTITUTION: A semiconductor integrated circuit device is composed of a titanium nitride film 12 and an aluminum film 13 formed on a substrate 1 where semiconductor devices are provided, a side wall protective film 19 formed on the side walls of the films 12 and 13, and an interlayer insulating film 20 provided covering the films 12 and 13, wherein a photoresist film serving as an etching mask is removed through a plasma ashing process where reactive gas composed of oxygen gas, carbon tetrafluoride, and nitrogen gas is used. By this setup, when plasma ashing takes place, a photoresist film is completely removed fully without etching a wiring film because an etching stop side wall protective film 19 is formed on the side wall of the wiring film.

31/7,DE/9 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04909221
METHOD OF FORMING ALUMINUM ALLOY WIRING

PUB. NO.: 07-201821 [JP 7201821 A]
PUBLISHED: August 04, 1995 (19950804)
INVENTOR(s): TAKII AKIMASA
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-337784 [JP 93337784]
FILED: December 28, 1993 (19931228)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PURPOSE: To provide a method of forming an aluminum alloy wiring by clean dry etching with high selectivity with an etching mask, protecting a side wall of a wiring in the etching, not generating after-corrosion and generating less particles.

CONSTITUTION: An aluminum alloy film 3 and a silicon oxide film 4 are formed on a BPSG2. Patterning the silicon oxide film 4 with a resist pattern 5, resist is removed. With a mask of the silicon oxide film 4, the aluminum alloy is dry etched by the plasma in a mixed gas that contains a chlorine gas and an oxygen gas. After this, forming alumina on an aluminum surface that has high etching selectivity with the mask and is chemically inert and etching the alumina, the side wall of the wiring is protected, anisotropical etching is done and the after-corrosion is prevented. By the use of the chlorine gas containing no carbon and by the elimination of the resist, a clean etching without carbon and with less generation of particles is provided.

31/7,DE/10 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

04836239
OPTICAL MASK AND ITS PRODUCTION

PUB. NO.: 07-128839 [JP 7128839 A]
PUBLISHED: May 19, 1995 (19950519)
INVENTOR(s): FUKUSHIMA YUICHI
APPLICANT(s): TOPPAN PRINTING CO LTD [000319] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-273847 [JP 93273847]
FILED: November 01, 1993 (19931101)
JAPIO CLASS: 29.1 (PRECISION INSTRUMENTS -- Photography & Cinematography); 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R004 (PLASMA)

ABSTRACT
PURPOSE: To eliminate a difference in transmittance between light transmissive parts and phase shift parts and to easily execute disposition for this purpose by correcting the intensity attenuation of the transmitted light of the light transmissive parts generated hitherto by the exposing light component inverted in phase by reflection by the side walls of the light transmissive parts so as to offset the attenuation.

CONSTITUTION: This process for production of the optical mask comprises forming an etching stop layer 22, a phase shift layer 23 and a light shielding layer 24 on a transparent substrate 21 and removing resists remaining after forming the light shielding layer patterns by applying photolithography, then forming phase shift layer patterns by overlap exposing to the light shielding layer patterns by applying the photolithography. The substrate is subjected to an oxidation treatment after formation of the phase shift layer patterns.

31/7,DE/11 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

04619197
FINE WORKING METHOD OF POLYIMIDE RESIN FILM

PUB. NO.: 06-291097 [JP 6291097 A]
PUBLISHED: October 18, 1994 (19941018)
INVENTOR(s): SHIMONE SUMISATO
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-079870 [JP 9379870]
FILED: April 06, 1993 (19930406)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 14.2 (ORGANIC CHEMISTRY -- High Polymer Molecular Compounds)
JAPIO KEYWORD: R004 (PLASMA); R044 (CHEMISTRY -- Photosensitive Resins)

ABSTRACT
PURPOSE: To form a forward taper on a contact hole section, and prevent the disconnection of an upper layer wiring, by a method wherein the dry etching of an layer insulating film is performed by using mixed gas of flon based gas and oxygen, and over etching is performed by using only oxygen gas when etching is ended.
CONSTITUTION: Polycrystalline silicon is deposited on a glass substrate 101, and a lower layer wiring 102 is obtained by patterning the silicon to be in a specific form. Polyimide resin as an layer insulating film 103 is spread and baked. Photoresist 104 is formed and used as the etching mask of

an layer insulating film 103, which is etched by using CHF(sub 3) gas and O(sub 2) gas. By observing the intensity change of SiF(sub 4) plasma light emission, the etching end point of the layer insulating film 103 is detected. When the lower layer wiring 102 under a part to be etched of the layer insulating film 103 is exposed, the intensity of SiF(sub 4) plasma light emission increases. From this time point, the supply of CHF(sub 3) gas is stopped, and over etching is performed by using only O(sub 2) gas.

31/7,DE/12 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

04275545
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 05-267245 [JP 5267245 A]
PUBLISHED: October 15, 1993 (19931015)
INVENTOR(s): HAYASHI HISATAKA
HORI MASARU
HORIOKA KEIJI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-063887 [JP 9263887]
FILED: March 19, 1992 (19920319)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R020 (VACUUM TECHNIQUES)

ABSTRACT
PURPOSE: To make it possible to form a silicon oxide film in a vertically specific configuration by using a heat-resistant thin film as a master mask when the silicon oxide film is etched.

CONSTITUTION: After a silicon oxide film 2 and a polysilicon thin film 3 are formed on a silicon substrate 1 in that order, a photoresist 4 is formed in a desired pattern. Then, after the polysilicon thin film 3 is vertically processed with the photoresist 4 as a mask, the remaining resist 4 is removed by a down flow ashing by use of a CF(sub 4)/O(sub 2), gas, for example, thereby to pattern the polysilicon thin film 3 on the silicon oxide film 2. Subsequently, while the silicon substrate 1 is kept at a given temperature of 120 deg.C or more almost constantly, the silicon oxide film 2 is etched anisotropically with the polysilicon thin film as a mask. In this way, it is possible to form the silicon oxide film 2 in a vertically specific configuration.

31/7,DE/13 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

03646665
SEMICONDUCTOR DEVICE

PUB. NO.: 04-011765 [JP 4011765 A]
PUBLISHED: January 16, 1992 (19920116)
INVENTOR(s): KOBAYASHI KEN
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-112636 [JP 90112636]
FILED: April 30, 1990 (19900430)

JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 45.2
(INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT
PURPOSE: To obtain a high electrostatic capacity without reducing in thickness a film by providing a dielectric film covering a conductor layer in electric contact with a reverse conductivity type region formed on the inner wall of a second groove.

CONSTITUTION: An SiO_2 film 2 is formed on a P-type silicon substrate 1 by a thermal oxidizing method, coated with photoresist 4 and formed in a desired shape. With the photoresist 4 as a mask the film 2 is patterned, and an element isolating groove 5 is opened by anisotropic dry etching. Then, an SiO_2 film 6 is deposited in the groove 5, a BPSG is further deposited, and anisotropically etched to form a substantially flat surface in the same plane as the surface of the substrate 1. A capacity groove is formed in a closed region surrounded by the conductor layer and the groove 5, and a second conductor layer in electric contact with the reverse conductivity type region formed on the inner wall is provided. When a third conductor phase is further provided on the second dielectric film covering the conductor layer, a high electrostatic capacity is obtained without reducing in thickness.

31/7,DE/14 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

02816441
FORMING METHOD FOR FINE PATTERN

PUB. NO.: 01-114041 [JP 1114041 A]
PUBLISHED: May 02, 1989 (19890502)
INVENTOR(s): TAKAHASHI SHIGERU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-272224 [JP 87272224]
FILED: October 27, 1987 (19871027)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS

ABSTRACT
PURPOSE: To form a fine pattern as compared with the limit resolution of an aligner by forming the pattern with the limit resolution of the aligner, and miniaturizing the pattern by isotropic etching.

CONSTITUTION: A silicon oxide film covering by thermal oxidation a silicon substrate 1 is selectively etched with a photoresist 3 as a mask, and a silicon oxide film 2 having the same width as that of the photoresist is formed. Then, the substrate 1 is dipped in a diluted fluoric acid to reduce the width of the film 2. Thereafter, after the resist 3 is removed, it is newly coated with resist, and etched by oxygen plasma thereby to expose the upper face of the film 2. Then, with a pattern 5 as a mask the substrate 1 is anisotropically etched to form a groove having 0.5.mu.m of width. Accordingly, a finer pattern than the limit resolution of the aligner can be formed.

31/7,DE/15 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

02797021
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 01-094621 [JP 1094621 A]
PUBLISHED: April 13, 1989 (19890413)
INVENTOR(s): MOTODO NOBUO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-252066 [JP 87252066]
FILED: October 05, 1987 (19871005)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PURPOSE: To prevent adhesion of matters on the surface of an aperture for decreasing defects of incompletely opened contacting apertures and to improve reliability of contact of interconnections, by using CF(sub 4) + O(sub 2) gas mixed at specific proportions fork the dry etching process for opening a contacting aperture in a silicon nitride film.

CONSTITUTION: An electrode interconnection 3 is provided selectively on an insulating film 2 on a semiconductor substrate 1. A silicon nitride film 4 is deposited on the surface including the electrode interconnection 3 and a photoresist film 5 having a pattern for providing contact for the electrode interconnection 3 is formed on the silicon nitride film 4. Then, the silicon nitride film 4 masked with the photoresist film 5 is dry etched with mixed gas of CF(sub 4) and O(sub 2) so that a contacting apertures 6 are opened. When a semiconductor device is produced in this manner, flow rate of the O(sub 2) in said mixed gas is controlled, for example, to be 30 to 50% of the total flow rate of the mixed gas of CF(sub 4) + O(sub 2) and anisotropic dry etching is performed with such CF(sub 4) + O(sub 2) gas, so that an aperture 7 having a cup-like cross section is formed. Following to peeling the photoresist film off, an aluminium interconnection 8 is provided.

31/7,DE/16 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

02727819
ETCHING

PUB. NO.: 01-025419 [JP 1025419 A]
PUBLISHED: January 27, 1989 (19890127)
INVENTOR(s): TATEIWA KENJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-181506 [JP 87181506]
FILED: July 21, 1987 (19870721)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PURPOSE: To perform anisotropic etching which is lacking in crosswise etching treatment and form a reproducible fine pattern by adding a

hydrocarbon gas in an oxygen gas and by etching an organic film in the plasma of the above mixed gas.

CONSTITUTION: A resist 4 is formed on a silicon oxide film 3 and the first opening 5 is formed through ordinary exposure and development process. The resist 4 is used as a mask and a silicon oxide film 3 is etched by performing reactive ion-etching with a CHF(sub 3) gas and then, the second opening 6 is formed. After using a mixed gas consisting of oxygen, a hydrocarbon gas, for example, CH(sub 4) gas, the third opening 7 is formed by etching an organic film 2 through a process of reactive ion-etching. In such a case, since the organic film 2 is etched while forming always a thin film of CH(sub x) at the side walls with the hydrocarbon gas in an etching gas, it is treated by anisotropic etching.

31/7,DE/17 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

02640349
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 63-257249 [JP 63257249 A]
PUBLISHED: October 25, 1988 (19881025)
INVENTOR(s): NAKADA SACHIKO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-092732 [JP 8792732]
FILED: April 14, 1987 (19870414)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)

ABSTRACT
PURPOSE: To obtain a semiconductor device whose characteristics are good by a method wherein one part of a substratum oxide film to be used as a field oxide film is etched in advance and a nitride film which is thicker than other parts is deposited on an edge part of the remaining substratum oxide film so that an active region is made wide and that miniaturization is realized.

CONSTITUTION: A substratum oxide film 2 is formed on one main face of a silicon substrate 1; the oxide film 2 is processed by an anisotropic plasma etching method by using a photolithographic technique by making use of a resist 5 as a mask. A nitride film 3 is formed on the oxide film 2; the nitride film 3 is coated with a resist 6. The resist 6 and the nitride film 3 are etched back at an identical rate; the surface of a thick part of the oxide film 2 is exposed. Then, the resist 6 is removed. The exposed substrate 1 is thermally oxidized by making use of the nitride film 3 as the mask; a field oxide film 4 is formed. By this setup, a semiconductor device whose characteristics are good can be obtained.

31/7,DE/18 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

02640348
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 63-257248 [JP 63257248 A]
PUBLISHED: October 25, 1988 (19881025)
INVENTOR(s): NAKADA SACHIKO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-092730 [JP 8792730]
FILED: April 14, 1987 (19870414)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)

ABSTRACT

PURPOSE: To obtain a semiconductor device whose characteristics are good by a method wherein one part of a substratum oxide film to be used as a field oxide film is formed to be thick in advance so that an active region is made wide and that miniaturization is realized.

CONSTITUTION: After a silicon substrate 1 has been thermally oxidized and a substratum oxide film 2 has been formed on the substrate 1, the oxide film 2 is processed to be a prescribed thickness by an anisotropic plasma etching method by using a photolithographic technique by making use of the oxide film 2 as a mask. A nitride film 3 is formed on the oxide film 2; the nitride film 3 is coated with a resist 6. The resist 6 and the nitride film 3 are etched at an identical etching rate; the surface of a thick part of the oxide film 2 is exposed. The remaining resist 6 is removed. The surface of the exposed oxide film 2 is thermally oxidized; a field oxide film 4 is formed. By this setup, a semiconductor device whose characteristics are good can be obtained.

31/7,DE/19 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

02604751
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 63-221651 [JP 63221651 A]
PUBLISHED: September 14, 1988 (19880914)
INVENTOR(s): ICHIKAWA MATSUO
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-054837 [JP 8754837]
FILED: March 10, 1987 (19870310)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)

ABSTRACT

PURPOSE: To suppress passing of oxygen atoms and to reduce bird's beaks, by providing a Si(sub x)N(sub y)O(sub z) film between a semiconductor substrate and a Si(sub 3)N(sub 4) film which serves as a mask material used to perform selective oxidation of a part in a surface region of a semiconductor substrate.

CONSTITUTION: A Bi(sub x)N(sub y)O(sub z) film 2 is formed 100 angstroms to 1500 angstroms on a semiconductor substrate 1 by a vapor growth method. Similarly, a Si(sub 3)N(sub 4) film 3 is formed 1000 angstroms to 3000 angstroms thereon by the vapor growth method. Next, a resist or the like is used as a mask to remove and etch the Si(sub 3)N(sub 4) film 3 selectively by Freon group plasma etching. This Si(sub 3)N(sub 4) film 3 with patterning finished is used as a mask to remove and etch the Si(sub x)N(sub y) O(sub z) film 2 selectively also by Freon group plasma etching. Next, stopper ion implantation is performed from above. Ions of the same polarity

as the semiconductor substrate 1 are used in this case. Thereafter, when the substrate is heated at 900 deg.C to 1100 deg.C for 4 to 5 hours or more in an atmosphere of oxygen or steam, or a mixture of them, a selective oxidizing film 4 is formed.

31/7,DE/20 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

01478026
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 59-189626 [JP 59189626 A]
PUBLISHED: October 27, 1984 (19841027)
INVENTOR(s): TSUKURA TAKASHI
OKUMA TORU
APPLICANT(s): MATSUSHITA ELECTRONICS CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-065055 [JP 8365055]
FILED: April 13, 1983 (19830413)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R044 (CHEMISTRY -- Photosensitive Resins)

ABSTRACT
PURPOSE: To form a contact hole which does not allow the dielectric strength of interlayer insulating film and has a high pattern size accuracy for tapered etching by using a first etching mask having a high etching characteristic and a second photo etching mask by the photo resist for an insulating film.
CONSTITUTION: A polycrystalline silicon 13 which becomes a first etching mask is formed at the surface of interlayer insulating film 12 on semiconductor substrate 11. The anisotropic etching is carried out to the polycrystalline silicon 13 using a photo resist film 14 and a first etching mask is formed by the polycrystalline silicon 13. Thereafter, a second etching mask 15 having a contact window which is smaller than that of the first etching mask 13 is formed using the photo resist film. The tapered etching is carried out to such a pattern having the etching masks 13, 15 in such a double-layer structure using the plasma obtained by adding oxygen gas to the fluorine gas plasma. Thereafter, the first and the second etching masks 13, 15 are removed and a tapered contact hole 16 can be obtained. An electrode of aluminium film 17 is formed on such hole.

31/7,DE/21 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO

00703443
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 56-023743 [JP 56023743 A]
PUBLISHED: March 06, 1981 (19810306)
INVENTOR(s): SASAKI ISAO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-099576 [JP 7999576]
FILED: August 03, 1979 (19790803)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R044 (CHEMISTRY -- Photosensitive Resins);

R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors, MOS)

ABSTRACT
PURPOSE: To contrive the reduction of a layer resistance of a diffused region and the enhancement of the density thereof in the semiconductor device by wiring Pt and Au on a diffused region.

CONSTITUTION: A polysilicon 4 is superposed on a field oxide film 2 and a gate oxide film 3 of a P-type Si substrate 1. A resist mask 5 is coated thereon to etch and to retain the polysilicon 4 in narrower width than the width of the mask. Then, the film 3 is etched, and Pt layer 6 and Au layer 7 are laminated thereon. The mask 5 is removed, and the surface of the gate layer 4 is oxidized to form an oxide layer 8. Thereafter, P ion is implanted thereto to form an N-type layer 9, and Si(sub 3)N(sub 4) mask 10 is coated theron, and the Pt layer and the Au layer are etched. Subsequently, an SiO(sub 2) film 11 is coated thereon, openings are selectively perforated thereat, aluminum electrodes 12 are wired thereon. This configuration can form partly the Pt film into platinum silicide to form an ohmic contact to prevent the Au from diffusing into the Si. The Au prevent oxidation. The SiO(sub 2) film 8 for enclosing the gate layer becomes a stopper of etching when perforating the openings at the Si(sub 3)N(sub 4) 10 so that the gate layer may not be short-circuited. Accordingly, the layer resistance is reduced to accelerate the operation and to increase the density.

31/7,DE/22 (Item 1 from file: 351)
DIALOG(R)File 351:DERWENT WPI

012202639
WPI Acc No: 99-008745/199901
Stacked capacitors with increased capacitance for DRAM cells - formed using chemical-mechanical polishing technology
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: TSENG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5834349	A	19981110	US 96755869	A	19961202	H01L-021/8242	199901 B

Priority Applications (No Type Date): US 96755869 A 19961202
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5834349	A		10			

Abstract (Basic): US 5834349 A
Fabricating stacked storage capacitors on a semiconductor substrate having device areas surrounded and electrically isolated from each other by field oxide areas. The device areas have semiconductor devices formed, in part, from a patterned polycide layer, and have device contact areas in the device areas. The substrate is coated with a first insulating layer having contact openings to the device contact areas. The method for fabricating stacked storage capacitors comprises depositing a first polysilicon layer on the substrate over the first insulating layer and electrically contacting the device contact areas, and planarising the polysilicon layer by chemical-mechanical polishing (CMP). A second insulating layer is deposited on the first polysilicon layer and patterned by photoresist masking and laterally recessing the

masking by isotropic plasma etching in oxygen to further reduce a min. feature size of the masking. The second insulating layer is anisotropically etched to leave portions having vertical sidewalls over the device contact areas where the stacked capacitors are to be formed. A third conformal insulating layer is deposited on the second insulating layer to provide a barrier to thermal oxidation, and anisotropically etched back to form sidewall spacers on the sidewalls of the patterned second insulating layer, and to further expose the first polysilicon layer elsewhere on the substrate. A polysilicon oxide is formed on the expose first polysilicon layer by thermal oxidation, and the sidewall spacers selectively removed thereby exposing the underlying first polysilicon layer. Trenches are formed in the first polysilicon layer by anisotropic plasma etching while using the second insulating layer and the polysilicon oxide as an etching mask, thereby forming inner sidewalls for bottom electrodes for the stacked capacitors. The second insulating layer and the polysilicon oxide are concurrently removed by wet etching. A patterned photoresist mask is formed having portions over the trenches thereby defining an outer perimeter of the bottom electrodes for an array of stacked capacitors. The first polysilicon layer is anisotropically plasma etched to the first insulating layer thereby forming the array of bottom electrodes having vertical sidewalls. An inter-electrode dielectric layer is formed on the bottom electrodes, and a second polysilicon layer deposited and patterned to form the top electrodes of the stacked storage capacitors.

USE - Method for fabricating an array of dynamic random access memory (DRAM) cells having stacked capacitors with increased capacitance using CMP technology.

ADVANTAGE - The stacked capacitors have bottom electrodes having portions extending vertically upward, thereby increasing capacitance, and formed using self aligning techniques in a cost effective manufacturing process.

Dwg.2,7/7

Title Terms: STACK; CAPACITOR; INCREASE; CAPACITANCE; DRAM; CELL; FORMING; CHEMICAL; MECHANICAL; POLISH; TECHNOLOGY
Derwent Class: L03; U11; U12; U13; U14
International Patent Class (Main): H01L-021/8242

31/7,DE/23 (Item 2 from file: 351)
DIALOG(R)File 351:DERWENT WPI

012139495
WPI Acc No: 98-556407/199847
Gate electrode and sidewall spacer manufacture for FET's - uses stacked gate electrode structure having TEOS oxide and nitride hard mask which minimises polymer build-up during patterning
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHANG T; CHOU C; TSAO J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5817562	A	19981006	US 97789212	A	19970124	H01L-021/336	199847 B

Priority Applications (No Type Date): US 97789212 A 19970124
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5817562	A		15			

Abstract (Basic): US 5817562 A

Gate electrode and sidewall spacer manufacture for field effect transistors (FETs) having self-aligned contacts (SAC) comprises: (a) providing a semiconductor substrate having device areas; (b) forming a gate oxide on the device areas; (c) depositing a conductively doped polysilicon layer on the device areas and on the substrate; (d) depositing a first insulating layer on the polysilicon layer; (e) depositing a hard mask layer on the first insulating layer; (f) patterning using a photoresist mask and anisotropic plasma etching the hard mask, the first insulating layer, and the first polysilicon layer, to form stacked gate electrode structures having vertical sidewalls over the device areas; (g) forming by ion implantation lightly doped source/drain areas in the device areas adjacent to the gate electrode structures; (h) growing by thermal oxidation a polysilicon oxide layer on sidewalls of the polysilicon layer in the stacked gate electrode structures, and concurrently on the lightly doped source/drain areas; (i) depositing a conformal first silicon nitride layer over the stacked gate electrode structures; (j) depositing a conformal second insulating layer on the first silicon nitride layer; (k) anisotropically plasma etching the second insulating layer and the first silicon nitride layer to form insulating sidewall spacers on the sidewalls of the stacked gate electrode structures, where the first silicon nitride layer remaining in the sidewall spacers is contiguous with the hard mask layer; (l) forming source/drain contact areas in the device areas adjacent to the insulating sidewall spacers by ion implantation; (m) depositing a blanket conformal second silicon nitride layer; (n) depositing a third insulating layer and annealing to form an essentially planar surface; (o) photoresist masking and selectively wet etching in the third insulating layer to the second silicon nitride layer to form openings extending partially over the stacked gate electrode structures, thus forming self-aligned source/drain contact openings over the source/drain contact areas; (p) plasma etching the second silicon nitride layer in the source/drain contact openings to the polysilicon oxide layer formed on the source/drain contact areas; (q) performing a pre-metal wet-etch dip to remove the polysilicon oxide, exposing the source/drain contact areas; and (r) depositing and patterning a metal layer to form electrical contacts to the source/drain contact areas.

ADVANTAGE - The silicon nitride minimises polymer build up during plasma etching. The vertical sidewalls of the gate electrode structure allow sidewall spacers to be formed with improved shape, i.e L-shaped, which prevents erosion of the of the TEOS oxide which can lead to electrical shorts between the source/drain metal contact and the polysilicon gate electrodes.

Dwg.7/8

Title Terms: GATE; ELECTRODE; SIDEWALL; SPACE; MANUFACTURE; FET; STACK; GATE; ELECTRODE; STRUCTURE; OXIDE; NITRIDE; HARD; MASK; MINIMISE; POLYMER ; BUILD; UP; PATTERN

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/336

31/7,DE/24 (Item 3 from file: 351)

DIALOG(R)File 351:DERWENT WPI

012077885

WPI Acc No: 98-494796/199842

Raised shallow trench isolation region manufacture for FET's - uses spin-on-glass to form disposable sidewall spacers on dielectric studs in

trenches, and wet etch-back
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: TSENG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5801082	A	19980901	US 97912322	A	19970818	H01L-021/76	199842 B

Priority Applications (No Type Date): US 97912322 A 19970818
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5801082	A		8			

Abstract (Basic): US 5801082 A
Fabricating raised shallow trench isolation regions in a semiconductor substrate, and gate electrodes for field effect transistors comprises: (a) forming a pad silicon oxide layer on the substrate; (b) depositing a silicon nitride layer on the pad oxide layer; (c) forming openings in the silicon nitride layer and the pad oxide layer surrounding device areas using a photoresist mask and anisotropic plasma etching; (d) removing the photoresist mask; (e) forming trenches by selectively anisotropic plasma etching the silicon substrate in the openings while leaving portions of the silicon nitride layer over the device areas; (f) forming a liner oxide by thermal oxidation on exposed surfaces of the trenches in the substrate; (g) forming a channel-stop implant in the trenches; (h) depositing a conformal gap-fill silicon oxide by CVD to fill the trenches; (i) chemical/mechanically polishing back the gap-fill silicon oxide to the silicon nitride layer; (j) removing the silicon nitride layer over the device areas, thereby forming raised dielectric studs in the trenches extending above the substrate surface; (k)

depositing a spin-on glass (SOG) by spin coating, thereby forming disposable SOG spacers on the raised dielectric studs; (l) curing the SOG by thermal annealing; (m) wet etching back the SOG and the pad oxide to the device areas while etching back the raised dielectric studs and the SOG spacers, thereby forming the shallow trench isolation regions having a convex raised surface relative to the substrate surface; (n) forming a gate oxide by thermal oxidation on the device areas; (o) depositing a polysilicon layer on the substrate; and (p) patterning the polysilicon layer and completing the gate electrodes for the field effect transistors.

ADVANTAGE - The FET threshold voltage characteristics are improved when the circuit is powered on. Using a wet etchback replaces CVD and plasma etchback, increasing the cost-effectiveness of the process.

Dwg.5,6/8
Title Terms: RAISE; SHALLOW; TRENCH; ISOLATE; REGION; MANUFACTURE; FET; FORM; DISPOSABLE; SIDEWALL; SPACE; DIELECTRIC; STUD; TRENCH; WET
Index Terms/Additional Words: FIELD; EFFECT; TRANSISTOR; SOG
Derwent Class: L03; U11
International Patent Class (Main): H01L-021/76

31/7,DE/25 (Item 4 from file: 351)
DIALOG(R)File 351:DERWENT WPI

012039240
WPI Acc No: 98-456150/199839
Stacked capacitor for DRAM - uses thermal oxidation and anisotropic oxidation to form the spacers followed by polishing and etching processes

to produce bottom electrodes with vertical portions
Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: TSENG H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5792693	A	19980811	US 97813721	A	19970307	H01L-021/8242	199839 B

Priority Applications (No Type Date): US 97813721 A 19970307
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5792693	A		13			

Abstract (Basic): US 5792693 A
A method of making stacked storage capacitors with bottom electrodes of increased surface area on semiconductor substrates comprises depositing and planarising an insulating layer (22) over the substrate (10) and isolated (12) device areas, depositing a silicon nitride layer (23) and etching node contact openings. Polysilicon node contacts are formed (24), a second nitride layer deposited, followed by a patterned photoresist masking layer, recessed areas formed and polysilicon oxide formed on the sides and bottom of the recess. Sidewall spacers are formed by anisotropic plasma etching, a second conformal polysilicon layer formed and chemical- mechanically polished to form studs. A second patterned photoresist mask is formed defining the outer perimeters of the bottom electrodes and the bottom electrodes with vertical portions are etched from the two polysilicon layers. An inter-electrode dielectric layer (36) is formed on the bottom electrode and a third polysilicon layer deposited and patterned to form the top electrode (38).

USE - As capacitors for high-density DRAMs

ADVANTAGE - Capacitance is increased in the same area, ground rule tolerances are minimised by self-alignment and only two masking steps are used to make the bottom electrode.

Dwg.11/11

Title Terms: STACK; CAPACITOR; DRAM; THERMAL; OXIDATION; ANISOTROPE; OXIDATION; FORM; SPACE; FOLLOW; POLISH; ETCH; PROCESS; PRODUCE; BOTTOM; ELECTRODE; VERTICAL; PORTION
Derwent Class: L03; U11; U12; U13; U14
International Patent Class (Main): H01L-021/8242

31/7,DE/26   (Item 5 from file: 351)
DIALOG(R)File 351:DERWENT WPI

011842181
WPI Acc No: 98-259091/199823
Forming copper dry etch hardmask - using silicon nitride and silica deposition on copper, before lithography and differential etch stopping at the silicon nitride layer
Patent Assignee: ANONYMOUS (ANON   )
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
RD 408077	A	19980410	RD 98408077	A	19980320	H01L-000/00	199823 B

Priority Applications (No Type Date): RD 98408077 A 19980320

Abstract (Basic): RD 408077 A

Copper dry etch is a new challenging technology. Providing an appropriate mask is also a challenge. Disclosed is a method for creating a Cu dry etch hard mask. The method is also compatible for subtractive Cu integration processes. Current processes use Ta or TaN on top of Cu as a protection layer. The Ta or TaN serves as oxide etch stop and will be exposed to the oxygen plasma and solvent used in resist strip step. These processes showed several issues such as corrosion, peeling and oxidation of Cu. The disclosed processing sequence to form a Cu dry etch hard mask is given below: 1. Cu dep, 2. SiN dep, 3. SiO2 dep, 4. Litho, 5. Differential etch, etch SiO2 and stop at SiN, 6. Resist strip, 7. SiN etch using SiO2 as mask and stops at Cu. The main benefit of using this approach is that resist can be removed while Cu is protected by SiN. The SiO2 and SiN thickness can be adjusted to accommodate integration requirement.

Title Terms: FORMING; COPPER; DRY; ETCH; HARD; MASK; SILICON; NITRIDE; SILICA; DEPOSIT; COPPER; LITHO; DIFFERENTIAL; ETCH; STOP; SILICON; NITRIDE; LAYER

Derwent Class: L03; U11

International Patent Class (Main): H01L-000/00

31/7,DE/27 (Item 6 from file: 351)

DIALOG(R)File 351:DERWENT WPI

011789673

WPI Acc No: 98-206583/199818

Manufacturing vertical walled stacked capacitor for DRAM cell - comprises using two photoresist masking steps and series of self aligning process steps

Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)

Inventor: TSENG H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5728617	A	19980317	US 96747501	A	19961112	H01L-021/8242	199818 B

Priority Applications (No Type Date): US 96747501 A 19961112

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5728617	A		11			

Abstract (Basic): US 5728617 A

Fabricating stacked storage capacitors on a semiconductor substrate comprises: (i) providing a semiconductor substrate having device areas surrounded and electrically isolated from each other by field oxide areas, the device areas having semiconductor devices formed, in part, from a patterned polycide layer, and having device contact areas in the device areas, the substrate coated with a first insulator layer having contact openings to the device contact areas; (ii) forming the stacked storage capacitors by depositing a first polysilicon layer on the substrate over the first insulating layer and electrically contacting the device contact areas; (iii) planarising the first polysilicon layer; (iv) depositing a second insulating layer on the first polysilicon layer; (v) photoresist masking and anisotropically etching openings having essentially vertical sidewalls in the second insulating layer to the first polysilicon layer over the device contact areas where the stacked capacitors are to be formed; (vi) depositing a conformal third insulating layer on the second insulating layer, the third insulating layer providing a barrier to thermal oxidation; (vii)

anisotropically etching back the third insulating layer, thereby forming sidewall spacers on the sidewalls of the openings in the second insulating layer and further exposing the first polysilicon layer in the openings; (viii) forming polysilicon oxide in the openings on the exposed first polysilicon layer by thermal oxidation; (ix) selectively removing the sidewall spacers, to expose the first underlaying polysilicon layer; (x) forming recessed areas in the first polysilicon layer by anisotropic plasma etching while using the second insulating layer and the polysilicon oxide as an etching mask, to form inner sidewalls for the stacked capacitors; removing concurrently the second insulating layer and the polysilicon oxide by wet etching; (xi) forming a patterned photoresist mask having portions over the recessed areas defining the outer perimeter of bottom electrodes for the array of stacked capacitors; (xii) anisotropic plasma etching the first polysilicon layer to the first insulating layer and thereby forming an array of bottom electrodes having vertical sidewalls; forming an inter:electrode dielectric layer on the bottom electrodes; (xiii) depositing a second polysilicon layer; and (xiv) patterning the second polysilicon layer to complete the stacked storage capacitors.

USE - Fabrication of an array of dynamic random access memory (DRAM) cells with vertical wall stacked capacitors.

ADVANTAGE - Increased capacitance; cost effective manufacturing process using only 2 photoresist masking steps and a series of self aligning techniques for making the capacitor bottom electrodes.

Dwg.9/9

Title Terms: MANUFACTURE; VERTICAL; WALL; STACK; CAPACITOR; DRAM; CELL; COMPRISE; TWO; PHOTORESIST; MASK; STEP; SERIES; SELF; ALIGN; PROCESS; STEP

Derwent Class: L03; U11; U12; U13; U14

International Patent Class (Main): H01L-021/8242

31/7,DE/28 (Item 7 from file: 351)

DIALOG(R)File 351:DERWENT WPI

011492145

WPI Acc No: 97-470051/199743

Fabrication of a dual gate dielectric module for memory having embedded logic - where photoresist does not come into contact with gate oxide layer reducing contamination of device

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)

Inventor: FANG C H; HUANG J; LIANG M; WANG C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5668035	A	19970916	US 96661259	A	19960610	H01L-021/70	199743 B

Priority Applications (No Type Date): US 96661259 A 19960610

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5668035	A		8			

Abstract (Basic): US 5668035 A

Fabricating a dual gate oxide for FET gate electrodes comprises a) forming field oxide regions on a semiconductor substrate surrounding and electrically isolating device areas; b) forming a gate oxide on device areas by thermal oxidation, and then polysilicon over the whole substrate; c) patterning the polysilicon by masking and anisotropic plasma etching leaving portions over a first device area and exposing

and removing by a wet etch the first gate oxide over a second device area; d) forming a second gate oxide layer by thermal oxidation on the second device area and at the same time a silicon oxide layer on the polysilicon, and then depositing a second polysilicon layer on them; e) patterning the second polysilicon layer leaving portions over the second device area and removing it to the oxide layer over the first device area; f) removing the silicon oxide on the first polysilicon layer using a wet etch and depositing an insulating layer on the first and second polysilicon layers; g) patterning and etching the insulating layer and at the same time the first and second polysilicon layers to complete the FET electrodes having first gate oxide over the first device area and second gate oxide over the second device area.

Also claimed is the method in which the device is a DRAM and the first device area is a memory cell and the second is a logic device.

USE - Fabrication of DRAM cells.

ADVANTAGE - Photoresist does not come into contact with the gate oxide layer reducing contamination of the device.

Dwg.9/9

Title Terms: FABRICATE; DUAL; GATE; DIELECTRIC; MODULE; MEMORY; EMBED; LOGIC; PHOTORESIST; CONTACT; GATE; OXIDE; LAYER; REDUCE; CONTAMINATE; DEVICE

Derwent Class: L03; U11; U13

International Patent Class (Main): H01L-021/70

31/7,DE/29 (Item 8 from file: 351)

DIALOG(R)File 351:DERWENT WPI

010988057

WPI Acc No: 96-485006/199648

Fabricating T-shaped capacitors in DRAM cells - by etching 1st and 2nd holes through insulating layer, depositing doped polysilicon@, etching back, etc.

Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)

Inventor: TSENG H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5567640	A	19961022	US 96583789	A	19960111	H01L-021/70	199648 B

Priority Applications (No Type Date): US 96583789 A 19960111

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5567640	A		11			

Abstract (Basic): US 5567640 A

A memory cell is fabricated by: (a) forming a barrier layer over a substrate and gate electrode, then forming an insulation layer; (b) forming a resist layer having an opening over the source; (c) etching a 1st hole defined by the opening, to a depth less than the thickness of the insulation layer; (d) laterally etching the resist with an O2 plasma to enlarge the 1st opening and form a 2nd opening over the source and concentric with the 1st hole; (e) anisotropically etching the 1st insulation layer and barrier layer using the etched resist as mask, and extending the 1st hole to expose the source, and etching through the 2nd opening to form a 2nd hole shallower than the 1st insulation layer thickness and defined by the sidewalls of the 1st insulation layer; (f) removing the resist and forming a 1st poly-Si layer completely filing the 1st and 2nd holes and covering the 1st

insulation layer; (g) etching back the poly-Si layer and removing it from the 1st insulating layer, then removing the 1st insulation layer using the barrier layer as an etch stop to form a T-shaped storage electrode; and (h) forming a dielectric layer and a top electrode over the storage electrode, then forming a top insulation layer over the substrate.

Also claimed is a method as above to mfr. T-shaped capacitor over a node in a substrate.

USE - The limitations of photographic techniques are overcome, the number of masking steps is reduced, and a capacitor can be formed with high density and capacitance. The mfr. is simple and inexpensive.

Dwg.9/9

Title Terms: FABRICATE; T-SHAPED; CAPACITOR; DRAM; CELL; ETCH; HOLE; THROUGH; INSULATE; LAYER; DEPOSIT; DOPE; POLY; SILICON; ETCH; BACK
Derwent Class: G06; L03; U11; U13; U14
International Patent Class (Main): H01L-021/70
International Patent Class (Additional): H01L-027/00

31/7,DE/30 (Item 9 from file: 351)
DIALOG(R)File 351:DERWENT WPI

010579329
WPI Acc No: 96-076282/199608
Prodn. of dynamic access memory capacitor having stacked capacitor of high capacitance - by multistage process involving oxide insulation mfr., dielectric layer formation, polysilicon@ formation, etching, doping, patterning etc.
Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: JENG J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
TW 264572	A	19951201	TW 94102861	A	19940401	H01L-029/92	199608 B

Priority Applications (No Type Date): TW 94102861 A 19940401
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
TW 264572	A		37			

Abstract (Basic): TW 264572 A

Mfr. of dynamic access memory capacitor having stacked capacitor with high capacitance comprises selectively forming heavy field oxide region on one semiconductor substrate, leaving active region for implementing as field effect device; forming one gate dielectric layer on substrate of the active region, depositing one first polysilicon layer on active region of the above field oxide region; removing part portion of the first polysilicon heavy layer, leaving part portion of the above active region as gate and part portion of the above field oxide region; forming source/drain structure on semiconductor substrate of two sides of the above active region gate; forming one first isolating layer on the above active and field oxide layer; defining the first isolating pattern on source/drain region, electrically contacting with the above stacked capacitor; implementing the above stacked capacitor; depositing one second polysilicon layer on active and field oxide region; depositing one second insulating layer on the above second polysilicon layer that at least comprises three thin films of Si_3N_4, spin-on glass coating film and chemical vapour deposited SiO_2; by anisotropic plasma etching technology etching back the second

isolating layer to remove the second isolating layer of flat region; defining photoresist pattern of capacitor region, removing the second isolating layer of unflat region by plasma etching technology; with the second isolating layer of the concave part above cell contact as etching mask, etching Si3N4 outside cell contact region, then selectively removing spin-on glass coating film and chemical vapour deposited SiO2 in the second isolating layer; with Si3N4 of cell contact concave part as oxidn. mask, oxidising exposed polysilicon, forming polysilicon thermal oxide, and removing Si3N4 of the concave part above cell contact; with the above polysilicon thermal oxide as etching mask, with anisotropic plasma etching technology etching part portion of the 2nd polysilicon layer; removing the polysilicon thermal oxide, and defining bottom plate pattern on left 2nd polysilicon layer; forming one capacitor dielectric layer on the bottom plate of the capacitor, depositing a 3rd polysilicon layer and patterning it as top plate of the stacked capacitor.

Dwg.0/22

Title Terms: PRODUCE; DYNAMIC; ACCESS; MEMORY; CAPACITOR; STACK; CAPACITOR; HIGH; CAPACITANCE; MULTISTAGE; PROCESS; OXIDE; INSULATE; MANUFACTURE; DIELECTRIC; LAYER; FORMATION; POLY; SILICON; FORMATION; ETCH; DOPE; PATTERN

Derwent Class: L03; U11; U12

International Patent Class (Main): H01L-029/92

International Patent Class (Additional): H01L-027/108

31/7,DE/31 (Item 10 from file: 351)

DIALOG(R)File 351:DERWENT WPI

010316901

WPI Acc No: 95-218159/199529

Optical mask manufacturing method for VLSI,ULSI - involves formation of etching stop layers from oxidation on exposure domain without involving phase shift layer pattern or shaded layer pattern

Patent Assignee: TOPPAN PRINTING CO LTD (TOPP)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 7128839	A	19950519	JP 93273847	A	19931101	G03F-001/08	199529 B

Priority Applications (No Type Date): JP 93273847 A 19931101

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 7128839	A		7			

Abstract (Basic): JP 7128839 A

The manufacturing method forms an etching stop layer (22) which is formed by the oxidation processing on a transparent substrate (21). A phase shift layer (23) is formed by the registration exposure to the shaded layer pattern. A shading layer (24) and a resist (25) are formed over the layered structure. By carrying out photolithography, the resist is removed leaving the shading layer.

By an electron beam patterning (27) and an electron beam registration patterning (28) followed by an oxygen plasma irradiation, the optical mask is formed containing the etching stop layer, phase shift layer and the shading layer. An exposure domain (22') where phase shift layer and shading layer are removed is subjected to oxidation.

ADVANTAGE - Simplifies method. Improves pattern resolution. Cancels difference in transmittivity and phase shift.

Dwg.3/4
Title Terms: OPTICAL; MASK; MANUFACTURE; METHOD; VLSI; FORMATION; ETCH; STOP; LAYER; OXIDATION; EXPOSE; DOMAIN; PHASE; SHIFT; LAYER; PATTERN; SHADE; LAYER; PATTERN
Derwent Class: G06; L03; P84; U11
International Patent Class (Main): G03F-001/08
International Patent Class (Additional): H01L-021/027

31/7,DE/32 (Item 11 from file: 351)
DIALOG(R)File 351:DERWENT WPI

009373692
WPI Acc No: 93-067171/199308
Self-aligned self-passivated heterojunction bipolar transistor - utilising a dual lift-off process to remove metal and dielectric simultaneously
Patent Assignee: ROCKWELL INT CORP (ROCW)
Inventor: ASBECK P M; CHANG M C F; HO W J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 5185274	A	19930209	US 91746259	A	19910815	H01L-021/265	199308 B

Priority Applications (No Type Date): US 91746259 A 19910815
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 5185274	A		11			

Abstract (Basic): US 5185274 A
A self-aligned and self-passivated heterojunction bipolar transistor process comprises: forming a semiconductor wafer including an undoped substrate, an N+GaAs subcollector layer over the substrate, a GaAs collector layer doped one type over the subcollector, a GaAs base layer doped a different type over the collector layer, an AlGaAs emitter layer doped the one type over the base layer, and a pair of cap layers, one over the emitter layer and the other over the one cap layer; forming a mesa for a single transistor consisting of the cap layers, emitter layer, base layer and part of the collector layer; planarising the mesa with insulation to isolate a single transistor; depositing a layer of photoresist at least over the mesa; forming a photoresist mask out of the photo-resist, characterised by an emitter region pedestal surrounded by an emitter peripheral region and a base contact region, by etching the photoresist through the cap layers to stop at the emitter layer; depositing a thin photo CVD layer of Si_3N_4 over the etched photoresist to cover the sidewalls of the pedestal, the sidewalls of the base contact region and the emitter peripheral region and base contact region; removing the Si_3N_4 from the top of the photoresist and the base contact region by using low pressure CF_4/O_2 plasma anisotropic RIE to preserve the side-wall Si_3N_4; selectively wet etching the base contact region to the base layer and depleting the emitter peripheral region AlGaAs under the Si_3N_4 to passivate the emitter peripheral region; proton damaging the collector region beneath the base contact region; depositing a base metal on the photoresist and in the base contact region; removing the photoresist and the photoresist top of the pedestal along with the Si_3N_4 affixed to it, and the base metal not used for the base contact; finishing a contact to the subcollector and a contact to the emitter, pref. an opening is etched through the insulation, and through the collector layer to the

subcollector layer, a collector contact metal is deposited in the opening and the metal isolated.

USE/ADVANTAGE - Production of self-aligned, self passivated advanced duel lift-off HBTs, which have low device parasitics and high current gains. For high fan-out gate arrays and high resolution ACDs.

(Dwg.8/11)

Title Terms: SELF; ALIGN; SELF; PASSIVATION; HETEROJUNCTION; BIPOLAR; TRANSISTOR; UTILISE; DUAL; LIFT-OFF; PROCESS; REMOVE; METAL; DIELECTRIC; SIMULTANEOUS

Derwent Class: L03; U11; U12

International Patent Class (Main): H01L-021/265

International Patent Class (Additional): H01L-029/70

31/7,DE/33 (Item 12 from file: 351)

DIALOG(R)File 351:DERWENT WPI

008064469

WPI Acc No: 89-329581/198945

Plasma etching of carbon film - anisotropically with hydrogen or oxygen, isotropically with fluoride gas, etc.

Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)

Number of Countries: 002 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 1246374	A	19891002	JP 8872891	A	19880326		198945 B
US 4975144	A	19901204	US 89324663	A	19890317		199051
US 5017264	A	19910521	US 90582769	A	19900914		199123
JP 2592284	B2	19970319	JP 8872891	A	19880326	C23F-004/00	199716

Priority Applications (No Type Date): JP 8872891 A 19880326; JP 8867573 A 19880322; JP 8867574 A 19880322

Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
JP 1246374	A		6			
US 4975144	A		15			
US 5017264	A		15			
JP 2592284	B2		5	Previous Publ.		JP 1246374

Abstract (Basic): JP 1246374 A

A carbon film of Vicker's hardness more than 2,000 kg/mm2 is etched by a plasma etching gas of hydrogen or oxygen anisotropically, of fluoride isotropically, or of hydrogen or oxygen added with fluoride to reduce etching speed.

ADVANTAGE - Shape of the etched carbon film is controlled.

Dwg.0/4

Abstract (Equivalent): US 5017264 A

Etching a C film comprises (a) placing the substrate contg. the C film in a reaction chamber, (b) supplying etchant gas contg. H2 and O2, (c) supplying electrical energy to excite the gas, and (d) etching at least a portion of the film using the excited etchant gas. A DC bias voltage may be applied to the substrate. The etching may be anisotropic.

ADVANTAGE - Improved removal of C. The method can be used to clean the inside of the chamber or the substrate holder. (15pp)

US 4975144 A

A pattern is formed in an amorphous carbon film by treating the unmasked zone with a plasma of nitrogen trifluoride or sulphur hexafluoride to remove the carbon in the treatment zone.

Pref. the mask is Si oxide, Si nitride or a photoresist. Pref. plasma is formed by applying high frequency radiation at a power level above 300 W.

ADVANTAGE - The method removes carbon without leaving solid deposits which can contaminate other areas of the substrate. Used for I.C. prodn. or for removing carbon deposits from inside CVD chambers. (15pp)h

Title Terms: PLASMA; ETCH; CARBON; FILM; ANISOTROPE; HYDROGEN; OXYGEN; ISOTROPIC; FLUORIDE; GAS
Derwent Class: L02; M14; P78
International Patent Class (Main): C23F-004/00
International Patent Class (Additional): B44C-001/22; C03C-015/00; C03C-025/06; H01L-021/62

31/7,DE/34 (Item 13 from file: 351)
DIALOG(R)File 351:DERWENT WPI

007856979
WPI Acc No: 89-122091/198916
Isolation structures for high density IC - with birds beak effect eliminated allowing closer device packing
Patent Assignee: IND TEC RES INST (INTE-N)
Inventor: CHAO F C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
US 4818235	A	19890404	US 88205558	A	19880607		198916 B

Priority Applications (No Type Date): US 8713012 A 19870210; US 88205558 A 19880607
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
US 4818235	A		7			

Abstract (Basic): US 4818235 A

A process for forming an isolation region for an IC comprises forming a poly-Si layer over this region on an Si substrate coated with a stree release on an Si substrate (10) coated with a stress-release layer (20), masking the isolation region and removing the unmasked part by dry etching, removing the mask and sequentially depositing an Si3N4 layer on the structure. The surface is then planarised with a photoresist layer, and both this and the nitride layer are anisotropically etched back to expose the top surface of the poly-Si (32). The residual photoresist is then removed and the poly-Si oxidised to form a field oxide layer, while the vertical surfaces remain masked with nitride. Pref. the stress release layer is a pad oxide layer, the Si substrate is p- or n-type, and etching is plasma or reactive ion etching. Pref. Si3N4 is deposited by LPCVD or PECVD and the structure is ion-implanted after etch back. Pref. the isolation region is used for a PMOS, NMOS or CMOS. Pref. after etch back and photoresist removal the structure is ion-implanted and the p-field mask removed. Pref. a semi-recessed field oxide is formed from the oxidised poly-Si and part of the substrate in the isolation region so that the thickness of the poly-Si needed to form the field oxide layer is reduced. Pref. the remaining nitride and stress-release layers are removed after the oxidn. step.

USE/ADVANTAGE - A method for defining isolation structures in ICs in which the patterned field oxide layer is free of bird's beak effect

is provided. Thus the transition region between active areas is minimised and higher packing densities may be obtained.
Title Terms: ISOLATE; STRUCTURE; HIGH; DENSITY; IC; BIRD; BEAK; EFFECT; ELIMINATE; ALLOW; CLOSE; DEVICE; PACK
Index Terms/Additional Words: INTEGRATE; CIRCUIT
Derwent Class: L03; U11
International Patent Class (Additional): H01L-021/76

31/7,DE/35 (Item 14 from file: 351)
DIALOG(R)File 351:DERWENT WPI

007812542
WPI Acc No: 89-077654/198911
Multilayer circuit for VLSI semiconductor element with dielectric - having polyimide levelling layer covered by thin non-hydroscopic silicon nitride layer
Patent Assignee: SIEMENS AG (SIEI)
Inventor: GSCHWANDTN A; KOKKOTAKIS N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
DE 3728348	A	19890309	DE 3728348	A	19870825		198911 B

Priority Applications (No Type Date): DE 3728348 A 19870825
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
DE 3728348	A		5			

Abstract (Basic): DE 3728348 A
Multilayer circuit for VLSI semiconductor elements has multilayer dielectric, consisting of a levelling polyimide layer covered by a thinner Si3N4 layer, between the metallisation planes and through-contacts with sloping sides. The novelty is that the sides of the through-contacts are completely covered with Si3N4.

The multilayer dielectric pref. consists of a levelling polyimide layer between 2 thinner Si3N4 layers. The circuit is produced by (a) applying and tempering the polyimide layer; (b) defining the through-contacts by a photoresist technique; (c) anisotropic etching of the contact holes in the polyimide layer with the photoresist structure as etching mask; (d) removal of the remaining mask; (e) deposition of Si3N4 over the entire surface; (f) anodic oxidn. of the Si3N4 layer in the areas where it covered the bottom of the contact holes (g) removal of the oxidised Si3N4 areas; and (h) application of the next metallisation plane.

The through-holes are made by reactive ion beam etching. The Si3N4 is produced by a plasma enhanced CVD process. Anodic oxidn. is carried out in an aq. electrolyte soln., using the substrate as anode., and the oxidised areas are removed by wet etching. An Al alloy with Si and Ti is used for metallisation. The thickness ratio of the polyimide and Si3N4 layers is 2-7. A first Si3N4 may be deposited over a first metallisation plane before stage (a).

USE/ADVANTAGE - The process is simple and ensures that the sides of the polyimide are completely covered by non-hygroscopic Si3N4, which prevents the polyimide absorbing water and reduces the flaw density in the polyimide layer.

5/6
Title Terms: MULTILAYER; CIRCUIT; VLSI; SEMICONDUCTOR; ELEMENT; DIELECTRIC; POLYIMIDE; LEVEL; LAYER; COVER; THIN; NON; HYDROSCOPIC; SILICON; NITRIDE;

LAYER
Index Terms/Additional Words: SCALE; INTEGRATE
Derwent Class: A23; A85; L03; U11
International Patent Class (Additional): H01L-021/88

31/7,DE/36 (Item 15 from file: 351)
DIALOG(R)File 351:DERWENT WPI

007660243
WPI Acc No: 88-294175/198842
Etching contact hole in double layer insulation - using only one photoresist on 1st inorganic and 2nd polymer layer by reactive ion etching with two gases, etc.
Patent Assignee: IBM CORP (IBMC)
Inventor: HORNER E; MUHL R; TRUMPP H
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week	
EP 286708	A	19881019	EP 87105700	A	19870416		198842	B
JP 63304644	A	19881212					198904	
US 4816115	A	19890328	US 88172738	A	19880323		198915	
EP 286708	B	19920122					199204	
DE 3776325	G	19920305					199211	
JP 93073338	B	19931014	JP 8832005	A	19880216	H01L-021/3205	199344	

Priority Applications (No Type Date): EP 87105700 A 19870416
Cited Patents: 6.Jnl.Ref; EP 227851; WO 8702179
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 286708	A	G	16			
Designated States (Regional): DE FR GB IT						
US 4816115	A		10			
EP 286708	B					
Designated States (Regional): DE FR GB IT						
JP 93073338	B		10	Based on		JP 63304644

Abstract (Basic): EP 286708 A
Prodn. of contact holes in double layer insulation involves : (a) applying a first inorg. insulating layer (IL-1) (7) to a substrate with a first metallisation (6); (b) applying a 2nd polymer insulating layer (IL-2) (8) to the first; (c) applying a positive photoresist (PR) (9) and precure; (d) selective exposure of the PR layer, then overall exposure and post-cure; (e) development of the PR with a basic developer; (f) reactive ion etching (RIE) with a first etching gas (G-1) of ca. 2/3 to 3/4 of IL-2 in the required contact hole areas exposed through the PR mask: (g) RIE with a second etching gas (G-2) for complete removal of IL-2, using IL-1 as etch stopper; (h) RIE with G-1 of Ca. 1/2 of IL-1; (i) RIE with G-2 to give a lateral shift of PR and IL-2 over the angle of the resist; (j) RIE with G-1 of the second half of IL-1; (k) RIE with G-2 to give a lateral shift of 14 and IL-2 over the angle of the resist; and (l) stripping of the residual PR.
Pref. IL-1 is a Si_3N_4 film produced by plasma deposition and conforming with all wafer topography and pref. is 0.2-0.8 micron thick. IL-2 is a planarising polyimide film applied by spin coating and pref. is 0.8-2 microns thick. PR is a 3-5 micron thick novolak film contg. a diazonaphthoquinone inhibitor. G-1 is CF_4 and G-2 O_2.
USE/ADVANTAGE - Only one mask is used to etch the holes in the double layer insulation. The technique is useful in the prodn. of IC

structures in VLSI technology.
6,7,8/10
Abstract (Equivalent): EP 286708 B
Method of making via holes in a double-layer insulation, comprising the following steps: (1) applying a first insulation layer (7) of inorganic material onto a substrate with a first metallurgy (6); (2) applying a second insulation layer (8) of polymeric material onto the first insulation layer (7); (3) applying a layer (3) of positive photoresist on the double layer (7, 8) and pre-baking; (4) image-wise exposure of the photoresist layer (9) and subsequent blanket exposure thereof, and post-baking; (5) developing the photoresist layer (9) with a basic developer; (6) reactive ion etching (RIE) with a first etching gas of approx. 2/3 to 3/4 of the second insulation layer (8) in the areas of the respective via holes exposed by the photoresist mask; (7) RIE with a second etching gas for completely removing the second insulation layer (8) in the areas exposed by the mask, with the first insulation layer (7) serving as an etch stop; (8) R
Abstract (Equivalent): US 4816115 A
Via holes are mad ein a double layer insulation by A) applying to a substrate with a 1st layer of metallurgy a 1st insulation layer (II), pref. a 0.2-0.8 micro Si3N4 layer, and then a 2nd IL of polymeric material, pref. a 0.8-2micro thick polyimide layer, B) applying a positive photoresist layer (PPL), pref. a 3-5 micro thick material based on novolak with a diazonaphthoquinone inhibitor and prebaking the assembly, C) imagewise and then blanketwise exposing the PPl, post baking the assembly and developing the PPL with a basic developer, D) reactive ion etching (RIE) 2/3 to 3/4 of the thickness of the 2nd IL in the areas of the respective via holes exposed by the mask using a 1st etching gas (EG) and RIE with a 2nd EG to completely remove the 2nd IL in the areas exposed by the mask with the 1st IL serving as etching stop, E) RIE with the 1st EG about half the thickness of the 1st IL and RIE with the 2nd EG to effect via the angle of the PPL a lateral shifting of the PPL and of the 2nd IL, F) RIE with the 1st EG the 2nd half of the 1st IL and RIE with the 2nd EG to effect via the angle of the PPL a lateral shifting of the PPL and of the 2nd IL and G) stripping residual PPL. ADVANTAGE - Only 1 mask is used saving a number of steps; a self aligned hole is obtd. through both IL with a better angle and a softer profile, which very positively influences the covering with a 2nd layer of metallurgy.
(10pp)
Title Terms: ETCH; CONTACT; HOLE; DOUBLE; LAYER; INSULATE; ONE; PHOTORESIST ; INORGANIC; POLYMER; LAYER; REACT; ION; ETCH; TWO; GAS
Derwent Class: A85; G06; L03; P78; P84; U11
International Patent Class (Main): H01L-021/3205
International Patent Class (Additional): B29C-037/00; B44C-001/22; C03C-015/00; C03C-025/06; G03F-007/20; H01L-021/302; H01L-021/31

31/7,DE/37 (Item 16 from file: 351)
DIALOG(R)File 351:DERWENT WPI

003873766
WPI Acc No: 84-019298/198404
Vertical-walled groove prodn. in silicon - esp. for electron beam transmission mask using three layer mask and reactive ion etching
Patent Assignee: IBM DEUT GMBH (IBMC)
Inventor: BEHRINGER U; GRESCHNER J; TRUMPP H J
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 98318	A	19840118	EP 82105957	A	19820703		198404 B
JP 59013329	A	19840124	JP 83109462	A	19830620		198409
US 4589952	A	19860520	US 84670463	A	19841109		198623
EP 98318	B	19870211					198706
DE 3275447	G	19870319					198712

Priority Applications (No Type Date): EP 82105957 A 19820703
Cited Patents: 2.Jnl.Ref; EP 12859; WO 8000639; EP 48291
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 98318	A	G	27			

Designated States (Regional): DE FR GB IT

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 98318	B	G				

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 98318 A

The Si substrate is given a first 2-9 micron thick photoresist coating, a second 0.1-0.2 micron Si_3N_4 coating and a third 0.2-0.5 microns outer coating of highly sensitive photoresist. The desired pattern is formed in the outer layer and transferred to the Si_3N_4 layer by reactive ion etching with CF_4 and to the first photoresist layer with O_2 at a pressure below 4 microbar. The grooves are produced by reactive ion etching in a CF_4 plasma with a very low F concn. through the window formed.

Pref. the first layer consists of diazoketone-sensitised phenol- or cresol- HCHO resin, PMMA, polyisoprene or polyimide. The Si_3N_4 layer is formed by plasma deposition. Pref. outer layer consists of diazoketone-sensitised phenol- or cresol-HCHO resin or PMMA.

Completely nontoxic CF_4 can be used for etching by selecting suitable materials for the individual layers. The process is used esp. for the prodn. of an electron beam mask (see fig.), in which grooves are etched in a B-doped Si layer on a Si substrate, the back of the substrate is etched away in an anisotropic etching process through a SiO_2 mask and the resultant structurised membrane of B-doped Si is coated with Au after removing the SiO_2 layer.

2E/3

Title Terms: VERTICAL; WALL; GROOVE; PRODUCE; SILICON; ELECTRON; BEAM; TRANSMISSION; MASK; THREE; LAYER; MASK; REACT; ION; ETCH
Index Terms/Additional Words: POLYPHENOL; CRESOL; RESIN; POLY; PMMA; METHYL ; POLYMETHACRYLATE; POLYISOPRENE; POLYIMIDE; POLYFORMALDEHYDE
Derwent Class: A89; G06; L03; P84; U11
International Patent Class (Additional): G03F-001/00; G03F-007/02; H01L-021/30

31/7,DE/38 (Item 17 from file: 351)
DIALOG(R)File 351:DERWENT WPI

003167324
WPI Acc No: 81-27866D/198116
Patterning metal wiring layer on semiconductor device - by forming aluminium layer on oxidised semiconductor, oxidising, applying aluminium, masking and etching
Patent Assignee: FAIRCHILD CAMERA CORP (FAIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
JP 55145357	A	19801112					198116 B

Priority Applications (No Type Date): US 7934782 A 19790430

Abstract (Basic): JP 55145357 A

An Al film is formed on a semiconductor device comprising SiO2 films formed on the surface of a semiconductor substrate having an impurity-doped region, and a layer of Si3N4 or nichrome having resistance to plasma etching. The Al film is oxidised to form an Al2O3 film having resistance to plasma etching. A thick Al film is formed on the Al2O3 film.

Masking layers of photoresist are formed on the thick Al film. The thick Al film is selectively plasma-etched using the Al2O3 film as an etching stopper.

Title Terms: PATTERN; METAL; WIRE; LAYER; SEMICONDUCTOR; DEVICE; FORMING; ALUMINIUM; LAYER; OXIDATION; SEMICONDUCTOR; OXIDATION; APPLY; ALUMINIUM; MASK; ETCH
Derwent Class: L03
International Patent Class (Additional): H01L-021/88

31/7,DE/39 (Item 18 from file: 351)
DIALOG(R)File 351:DERWENT WPI

002248282
WPI Acc No: 79-47478B/197926
Plasma etching of silica - on a semiconducting silicon substrate, using carbon tetrafluoride and oxygen mixt.
Patent Assignee: IBM CORP (IBMC)
Inventor: CLARK H A
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
EP 2503	A	19790627					197926 B
JP 54086482	A	19790710					197934
US 4180432	A	19791225					198002
EP 2503	B	19820428					198218
DE 2861773	G	19820609					198224

Priority Applications (No Type Date): US 77861796 A 19771219
Cited Patents: DE 2703659; FR 2240526; US 3867216; 4.Jnl.Ref
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
EP 2503	A	G				
Designated States (Regional): DE FR GB						
EP 2503	B	G				
Designated States (Regional): DE FR GB						

Abstract (Basic): EP 2503 A

Method of etching SiO2, esp. a layer of SiO2 on a semiconductor substrate, is claimed, in which a plasma contg. 5-15 (10) vol. % CF4 balance O2 is used at a pressure of 1 Torr. The SiO2 is masked off using Si3N4 to form a window of exposed SiO2 of predetermined shape and size, prior to plasma etching. Alternatively, the mask is formed using an organic photoresist and Si3N4, the organic photoresist being removed with the SiO2 by etching.

Within the given range of plasma gas compsn. the SiO2 is etched faster than Si, so that it is not necessary to stop plasma etching before the si is reached as in prior art when the plasma gas contained fluorohydrocarbons and O2.

Title Terms: PLASMA; ETCH; SILICA; SEMICONDUCTOR; SILICON; SUBSTRATE; CARBON; TETRA; FLUORIDE; OXYGEN; MIXTURE
Derwent Class: L03; P78; U11; U12
International Patent Class (Additional): B44C-001/22; C03C-015/00; C03C-025/06; C23C-015/00; H01L-021/26

32/TI/1 (Item 1 from file: 2)
DIALOG(R)File 2:

Title: Reactive ion etching of semiconductor materials and of dielectric and metal layers

32/TI/2 (Item 1 from file: 8)
DIALOG(R)File 8:

Title: Removal of titanium oxide grown on titanium nitride and reduction of via contact resistance using a modern plasma asher

32/TI/3 (Item 1 from file: 347)
DIALOG(R)File 347:

METHOD FOR MANUFACTURING DIELECTRIC ELEMENT

32/TI/4 (Item 2 from file: 347)
DIALOG(R)File 347:

MANUFACTURE OF SEMICONDUCTOR DEVICE

32/TI/5 (Item 3 from file: 347)
DIALOG(R)File 347:

SEMICONDUCTOR DEVICE

32/TI/6 (Item 4 from file: 347)
DIALOG(R)File 347:

COMPOUND SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

32/TI/7 (Item 5 from file: 347)
DIALOG(R)File 347:

FORMING METHOD OF FINE PATTERN

32/TI/8 (Item 6 from file: 347)
DIALOG(R)File 347:

METHOD FOR FORMING PATTERN

32/TI/9 (Item 7 from file: 347)
DIALOG(R)File 347:

MANUFACTURE OF THIN-FILM INTEGRATED CIRCUIT DEVICE

32/TI/10 (Item 8 from file: 347)

MANUFACTURE OF SEMICONDUCTOR DEVICE

32/TI/11 (Item 9 from file: 347)

MANUFACTURE OF SEMICONDUCTOR DEVICE

32/TI/12 (Item 1 from file: 351)

Corrosion preventing method for metal interconnection in IC - includes depositing aluminium@-copper@ alloy layer, covering the photoresist, reacting etching the layer, soaking the semiconductor substrate chip, etc.

32/TI/13 (Item 2 from file: 351)

Oligomerised cyclo-butarene resins of specified mol. wt. - used in photo-definable compsns. for electronics applications.

32/TI/14 (Item 3 from file: 351)

Pattern etching a film of lead zirconium titanium oxide material - by pattern masking the film and dry plasma etching pref. using halogenated gas mixt., to give a very accurate and selective pattern etch

32/TI/15 (Item 4 from file: 351)

Photolithographic patterning of reflective metal layer - by using partially oxidised titanium@ as anti-reflection coating

32/TI/16 (Item 5 from file: 351)

Self-aligned interconnect fabrication process - uses copper@-polyimide to give versatile packaging without need for multiple layers

32/TI/17 (Item 6 from file: 351)

Forming thin film resistor on IC wafer - by forming patterned resistive layer with overlying protective layer formed by sputter etching

32/TI/18 (Item 7 from file: 351)

Forming dielectric film on substrate - by depositing soln. of cyclo-silazane polymer and spinning, esp. in mfr. of integrated circuits

32/TI/19 (Item 8 from file: 351)

Lift-off mask with defect-free oxygen barrier layer - formed by plasma polymerisation of silane, silazane and siloxane monomers
?pause
?t s32/7,de/1,3,4,6,7,8,9,10,17

32/7,DE/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

03315865 INSPEC Abstract Number: B89015757
Title: Reactive ion etching of semiconductor materials and of dielectric and metal layers
Author(s): Novotny, Z.
Author Affiliation: TESLA Electron. Res. Inst., Prague, Czechoslovakia
Journal: TESLA Electronics vol.19, no.3-4 p.59-62
Publication Date: Dec. 1986 Country of Publication: Czechoslovakia
CODEN: TNPTAQ ISSN: 0563-1823
Language: English Document Type: Journal Paper (JP)
Treatment: Experimental (X)
Abstract: In an effort to obtain micron and submicron dimensions of transistor and IC patterns, plasma etching techniques are widely used for the transfer of masks produced on various types of metal and dielectric layers by lithography. Etching of SiO/sub 2/, Si/sub 3/N/sub 4/, Ti-W and AZ 1350H layers as well as of Si single crystals and GaAs in pure CF/sub 4/ was carried out in an RIE (reaction ion etching) equipment. The AZ 1350H photoresist layers were, moreover, etched in pure O/sub 2/. Besides the dependence of etch rates on the parameters of the etching process (pressure, power), the process of sputtering brought about by the bombardment of GaAs in CF/sub 4/ and O/sub 2/ and of SiO/sub 2/ in O/sub 2/ was investigated. (17 Refs)
Descriptors: gallium arsenide; integrated circuit technology; metallisation; photoresists; semiconductor technology; silicon; silicon compounds; sputter etching; titanium alloys; tungsten alloys

32/7,DE/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05637178
METHOD FOR MANUFACTURING DIELECTRIC ELEMENT

PUB. NO.: 09-251978 [JP 9251978 A]
PUBLISHED: September 22, 1997 (19970922)
INVENTOR(s): FUJII SATORU
TAKAYAMA RYOICHI
KAMATA TAKESHI
TOMOSAWA ATSUSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 08-060515 [JP 9660515]
FILED: March 18, 1996 (19960318)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 12.6 (METALS -- Surface Treatment)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce damages of photoresist and to stop generating residue on a film forming substrate or an electrode film by a method wherein, after patterning of a dielectric is etched with a hydrogen fluoride acid and oxidizing agent, a preprocessing is performed with reducing agent and continuously a postprocessing is performed with an acid.

SOLUTION: A lower metal electrode film 102, a dielectric film 103 and an upper metal electrode film 104 are sequentially formed on a substrate 101. Continuously, by use of the patterned upper metal film 104 as a mask, the dielectric film 103 is patterned by chemical etching. As an etchant, a substance that oxidizing agent is added to a hydrogen fluoride acid solution is used. It is impregnated in preprocessing liquid of a composition having a volume ratio of a sulfite solution to an acetic acid which is about 1 to 5. Thereafter, it is impregnated in postprocessing liquid of a composition of about 5mol/l of hydrochloric acid, and a dielectric film and etching residue are completely etched.

32/7,DE/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03027726
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 02-003226 [JP 2003226 A]
PUBLISHED: January 08, 1990 (19900108)
INVENTOR(s): FUJITA KAZUYOSHI
AZUMA MASAHIKO
MATSUMURA HIDEAKI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-151560 [JP 88151560]
FILED: June 20, 1988 (19880620)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R100 (ELECTRONIC MATERIALS -- Ion Implantation)

ABSTRACT

PURPOSE: To prevent dielectric breakdown of a thin insulating film by separately placing resist masks to be used for patterning in the region on a thick insulating film and the region on a thin insulating film during the time of dry etching.

CONSTITUTION: For instance, a thick field insulating film 2 is formed on an n-type semiconductor substrate 1 by a selective oxidation method, while next forming a gate insulating film 3. A doped polycrystalline silicon layer 4 is all over formed, a resist mask 51 is formed in the gate electrode formation region and a resist mask 61 is formed in the capacitor electrode plate region being separated from the resist mask 51. Next, a polycrystalline silicon layer 4 is patterned by a plasma etching method performing by using carbon tetrafluoride gas or the like so as to form a gate electrode 5 and a capacitor plate 6 mutually separately. Next, the resist masks 51 and 56 are removed by ashing. That is, charge density of a conductor layer 4 formed on the thin insulating film 3 through the resist

masks 51 and 61 is not undesirably raised so that dielectric breakdown of the thin insulating film is excluded.

32/7,DE/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

02091674
COMPOUND SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 62-008574 [JP 62008574 A]
PUBLISHED: January 16, 1987 (19870116)
INVENTOR(s): MAEDA MUNEO
HAIRI ISAMU
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-147352 [JP 85147352]
FILED: July 04, 1985 (19850704)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R004 (PLASMA); R095 (ELECTRONIC MATERIALS -- Semiconductor Mixed Crystals)

ABSTRACT

PURPOSE: To obtain an FET characterized by excellent dielectric strength of a gate and high performance, by forming an insulating film, wherein aluminum oxide and an oxide film, which is a oxidized high-concentration cap layer therebelow, are formed, on the side surface of an aluminum gate, and isolating the gate.

CONSTITUTION: On an Si-GaAs substrate 10, an Si-GaAs layer 1 and an n-GaAlAs layer 2 are formed. After an SiO(sub 2) film 4 is deposited, etching is performed with a resist film pattern 11 as a mask, and the layer 2 is exposed. A part of an n(sup +)-GaAs layer 3 is exposed. Then, an aluminum film 5 and an aluminum film 5' are evaporated and deposited. Thereafter, the unnecessary parts of the aluminum films 5 and 5' and the resist film pattern 11 are lifted off together and removed. Then, with this SiO(sub 2) film 4 as a mask, the aluminum film 5' is oxidized by an oxidizing method using microwave exciting oxygen plasma, and an Al(sub 2)O(sub 3) film 15 is grown. Thereafter source and drain electrodes 6 are formed, and the hetero-junction FET is completed.

32/7,DE/7 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01587932
FORMING METHOD OF FINE PATTERN

PUB. NO.: 60-066432 [JP 60066432 A]
PUBLISHED: April 16, 1985 (19850416)
INVENTOR(s): SUGITA AKIO
HIKITA MAKOTO
TAMAMURA TOSHIAKI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-174197 [JP 83174197]
FILED: September 22, 1983 (19830922)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 14.2 (ORGANIC

CHEMISTRY -- High Polymer Molecular Compounds)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PURPOSE: To obtain a flattened fine pattern by providing a process, etc. in which a thin-film on a resist pattern is removed through a lift-off method in a solvent capable of dissolving an organic high molecular material film. CONSTITUTION: An organic high molecular material film 22 as a lower layer is applied on a substrate 1 and an organic metallic negative type resist 23 as an upper layer, beams, electron rays or X-rays are projected in a pattern shape, and a resist pattern is formed through development. The organic high molecular material film 22 is patterned by using oxygen gas plasma etching while employing the resist pattern as a mask. The upper section of the pattern of the film 22 is coated with a thin-film 3 consisting of a metal, a semiconductor or a dielectric through evaporation, etc., and a pattern of the thin-film is obtained through a lift-off method by using a solvent for the organic high molecular material film. When the pattern of the thin-film is flattened, the organic high molecular material film 22 is patterned, the substrate is patterned through plasma etching, an etched depth section is coated with the thin-film, and the thin-film pattern is formed through the lift-off method.

32/7,DE/8 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

01581234
METHOD FOR FORMING PATTERN

PUB. NO.: 60-059734 [JP 60059734 A]
PUBLISHED: April 06, 1985 (19850406)

INVENTOR(s): HORAI MASATAKA
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 58-168603 [JP 83168603]
FILED: September 13, 1983 (19830913)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 29.1 (PRECISION INSTRUMENTS -- Photography & Cinematography)
JAPIO KEYWORD:R004 (PLASMA)

ABSTRACT

PURPOSE: To prevent difference in pattern size conversion and deterioration of resolution associated with it which inhibit patterns from being formed with single-layered resist on an integrated circuit having uneveness, by selectively removing a radioactive-ray-sensitive resin film of the first layer through the reduced silver patterns converted from a silver halide emulsion film of the second layer.

CONSTITUTION: Positive-type ultraviolet resist 7 is appled on a substrate 1 over a covering film 2 such as a distribution or dielectric layer having a level difference patterns 2a such that the resist has a thickness larger than the level difference of the pattern 2a. The resist film 7 is then hardened by soft baking. Silver halide emulsion 8 is further applied over there, and then the second layer of silver halide emulsion film 8 is selectively radiated through a mask 9 with the light 10 of a proper wavelength range. Development and fixation are applied thereto for converting the latent image pattersn 8a into reduced silver patterns 8b to dissolve and removed the non-exposed portion of the silver halide emulsion film 8. The first layer of resist 7 is etched in the atmosphere of oxygen

gas plasma to form resist patterns 7a.

32/7,DE/9 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

01452252
MANUFACTURE OF THIN-FILM INTEGRATED CIRCUIT DEVICE

PUB. NO.: 59-163852 [JP 59163852 A]
PUBLISHED: September 14, 1984 (19840914)
INVENTOR(s): YOSHIDA SHINJI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-038532 [JP 8338532]
FILED: March 09, 1983 (19830309)
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components); 42.1 (ELECTRONICS -- Electronic Components)
JAPIO KEYWORD:R004 (PLASMA); R044 (CHEMISTRY -- Photosensitive Resins)

ABSTRACT

PURPOSE: To miniaturize the titled device, to increase a scale for integration and to improve economical efficiency by forming a tantalum group oxide film on a tantalum nitride film shaped on a substrate and selectively removing the tantalum group oxide film.

CONSTITUTION: A tantalum nitride film 12 and a tantalum nitride oxide film 13 are formed continuously on a substrate 11, a photo-resist film 14 is formed, and the film 13 and the film 12 are etched selectively while using a pattern of the film 14 as a mask. A dielectric pattern is shaped, and the film 13 is removed selectively to the film 12 while employing the resist pattern of the dielectric pattern as a mask. The film 13, a section in the vicinity of the interface between the film 13 and the film 12, etc. are oxidized through an anodic oxidation method, and a dielectric film 15 for a capacitor is completed. A conductor pattern containing an upper electrode for the capacitor is formed. Accordingly, the stability of a resistance value adjusting process is improved because the reproducibility of the thickness of the film 12 is excellent.

32/7,DE/10 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

01339975
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 59-051575 [JP 59051575 A]
PUBLISHED: March 26, 1984 (19840326)
INVENTOR(s): ISHIKAWA OSAMU
EZAKI TAKEYA
KUBOTA MASABUMI
NISHIZAWA JUNICHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
SEMICONDUCTOR RES FOUND [351933] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-162499 [JP 82162499]
FILED: September 17, 1982 (19820917)

JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD:R100 (ELECTRONIC MATERIALS -- Ion Implantation); R132 (ELECTRONIC MATERIALS -- Electrostatic Induction Type Transistors, SIT)

ABSTRACT

PURPOSE: To increase dielectric resistance between a gate and a source, to improve a voltage amplification factor and to augment currents by providing a process, in which a thermal oxide film is formed and removed, a gate forming process and a source forming process.

CONSTITUTION: An underlay oxide film 14 is formed on an N type epitaxial layer 12a, a nitride film 13 is deposited, only the nitride film 13 is patterned by using plasma etching, and thick oxide films 15 in approximately 1-2.mu.m are formed by using a method such as oxidation at high pressure. When the oxide films 15 and the nitride film 13 are removed extending over the whole surface, projected sections 17 to which the sources are formed and recessed sections 16 to which the gates are formed can be formed to the N type epitaxial layer 12a. Sections as source regions are coated with resists 18 as masks for ion implantation, P(sup +) type impurity regions 19 are formed on the bottoms of the recessed sections 16, and the regions 19 are diffused up to predetermined channel width 23 through heat treatment to form gates 20. Nitride films 21 are left on the source regions and the gates 20, oxide films 22 are formed to the side surfaces of the recessed sections, and the N(sup +) type sources 25 are formed under the projected sections through a method such as ion implantation.

32/7,DE/17 (Item 6 from file: 351)
DIALOG(R)File 351:DERWENT WPI

008736778
WPI Acc No: 91-240794/199133
Forming thin film resistor on IC wafer - by forming patterned resistive layer with overlying protective layer formed by sputter etching
Patent Assignee: ANALOG RES & DEV LT (ANAL-N)
Inventor: BAIN A D; LANE W A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
GB 2240875	A	19910814	GB 9022632	A	19901018		199133 B

Priority Applications (No Type Date): IE 90458 A 19900212
Patent Details:

Patent	Kind	Lan	Pg	Filing Notes	Application	Patent
GB 2240875	A		41			

Abstract (Basic): GB 2240875 A

Resistor is formed on an IC wafer by depositing resistive material; adding a protective layer of conductive material; patterning the latter through a photoresist mask; and removing exposed resistive layer by RF sputter -etching. The protective layer is pref. a 150-1000 Angstrom, more pref. a 400-1000 Angstrom, layer of Ti and/or W, esp. an alloy of 90% Ti and 10% W. The resistive layer is pref. SiCr, NiCr or TaN, esp. SiCr.

The photoresist mask is removed before the RF sputter etch. The protective layer is patterned by etching through the photoresist mask most, pref. all, of the exposed protective layer being removed. The

etching may be a dry etch, esp. a CF4/O2 plasma, or a wet H2O2 etch at 40-60 deg.C. The sputter etch is performed in a non-reactive atmos. pref. Ar, at a self-bias of 1600 V for 30 m The resistor layer is a 20-60 Angstrom layer deposited by sputtering.

ADVANTAGE - Risk of damage to the resistor during subsequent wafer processing is reduced. An interconnect pattern, pref. of 4-40 k Angstrom Al, is then added; a diffusion barrier layer, pref. of 500-1500 Angstrom W alloy, is pref. included between substrate and Al. Remaining exposed diffusion barrier and protective layers may then be removed. The wafer may be post heat-treated at up to 250 deg.C. The wafer may include MOS and/or bipolar devices, the resistor(s) having being deposited on a surface passivation dielectric layer.

Dwg.2,4/9

Title Terms: FORMING; THIN; FILM; RESISTOR; IC; WAFER; FORMING; PATTERN; RESISTOR; LAYER; OVERLIE; PROTECT; LAYER; FORMING; SPUTTER; ETCH

Index Terms/Additional Words: INTEGRATE; CIRCUIT

Derwent Class: G06; L03; M14; U11; U14

International Patent Class (Additional): H01C-007/00